

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT368**

Hex buffer/line driver; 3-state;  
inverting

Product specification  
File under Integrated Circuits, IC06

December 1990

## Hex buffer/line driver; 3-state; inverting

## 74HC/HCT368

## FEATURES

- Inverting outputs
- Output capability: bus driver
- $I_{CC}$  category: MSI

The 74HC/HCT368 are hex inverting buffer/line drivers with 3-state outputs. The 3-state outputs ( $\overline{nY}$ ) are controlled by the output enable inputs ( $\overline{1OE}$ ,  $\overline{2OE}$ ).

A HIGH on  $\overline{nOE}$  causes the outputs to assume a high impedance OFF-state.

The “368” is identical to the “367” but has inverting outputs.

## GENERAL DESCRIPTION

The 74HC/HCT368 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f = 6\text{ ns}$

| SYMBOL            | PARAMETER                                | CONDITIONS                                   | TYPICAL |     | UNIT |
|-------------------|------------------------------------------|----------------------------------------------|---------|-----|------|
|                   |                                          |                                              | HC      | HCT |      |
| $t_{PHL}/t_{PLH}$ | propagation delay nA to $\overline{nY}$  | $C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$ | 9       | 11  | ns   |
| $C_I$             | input capacitance                        |                                              | 3.5     | 3.5 | pF   |
| $C_{PD}$          | power dissipation capacitance per buffer | notes 1 and 2                                | 30      | 30  | pF   |

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz

$f_o$  = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in V

2. For HC the condition is  $V_I = \text{GND to } V_{CC}$   
For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

## ORDERING INFORMATION

See “74HC/HCT/HCU/HCMOS Logic Package Information”.

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PIN DESCRIPTION

| PIN NO.             | SYMBOL                             | NAME AND FUNCTION                 |
|---------------------|------------------------------------|-----------------------------------|
| 1, 15               | $\overline{1OE}, \overline{2OE}$   | output enable inputs (active LOW) |
| 2, 4, 6, 10, 12, 14 | 1A to 6A                           | data inputs                       |
| 3, 5, 7, 9, 11, 13  | $1\overline{Y}$ to $6\overline{Y}$ | data outputs                      |
| 8                   | GND                                | ground (0 V)                      |
| 16                  | V <sub>CC</sub>                    | positive supply voltage           |



## Hex buffer/line driver; 3-state; inverting

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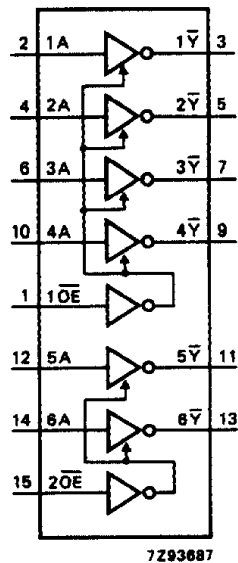


Fig.4 Functional diagram.

## FUNCTION TABLE

| INPUTS           |    | OUTPUTS         |
|------------------|----|-----------------|
| $\overline{nOE}$ | nA | $n\overline{Y}$ |
| L                | L  | H               |
| L                | H  | L               |
| H                | X  | Z               |

### Note

1. H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
Z = high impedance OFF-state

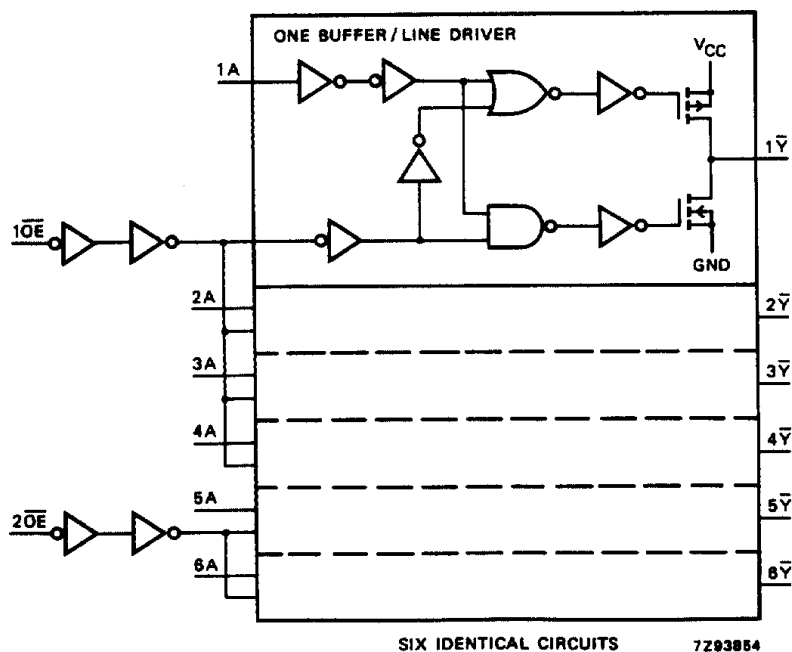


Fig.5 Logic diagram.

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**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

| SYMBOL                              | PARAMETER                                                       | T <sub>amb</sub> (°C) |                |                 |            |                 |             |                 | UNIT | TEST CONDITIONS        |           |
|-------------------------------------|-----------------------------------------------------------------|-----------------------|----------------|-----------------|------------|-----------------|-------------|-----------------|------|------------------------|-----------|
|                                     |                                                                 | 74HC                  |                |                 |            |                 |             |                 |      | V <sub>CC</sub><br>(V) | WAVEFORMS |
|                                     |                                                                 | +25                   |                |                 | −40 to +85 |                 | −40 to +125 |                 |      |                        |           |
|                                     |                                                                 | min.                  | typ.           | max.            | min.       | max.            | min.        | max.            |      |                        |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>nA to n $\bar{Y}$                          |                       | 30<br>11<br>9  | 95<br>19<br>16  |            | 120<br>24<br>20 |             | 145<br>29<br>25 | ns   | 2.0<br>4.5<br>6.0      | Fig.6     |
| t <sub>PZH</sub> / t <sub>PZL</sub> | 3-state output enable time<br>n $\overline{OE}$ to n $\bar{Y}$  |                       | 41<br>15<br>12 | 150<br>30<br>26 |            | 190<br>38<br>33 |             | 225<br>45<br>38 | ns   | 2.0<br>4.5<br>6.0      | Fig.7     |
| t <sub>PHZ</sub> / t <sub>PLZ</sub> | 3-state output disable time<br>n $\overline{OE}$ to n $\bar{Y}$ |                       | 55<br>20<br>16 | 150<br>30<br>26 |            | 190<br>38<br>33 |             | 225<br>45<br>38 | ns   | 2.0<br>4.5<br>6.0      | Fig.7     |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time                                          |                       | 14<br>5<br>4   | 60<br>12<br>10  |            | 75<br>15<br>13  |             | 90<br>18<br>15  | ns   | 2.0<br>4.5<br>6.0      | Fig.6     |

## Hex buffer/line driver; 3-state; inverting

## 74HC/HCT368

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT             | UNIT LOAD COEFFICIENT |
|-------------------|-----------------------|
| 1 $\overline{OE}$ | 1.00                  |
| 2 $\overline{OE}$ | 0.90                  |
| nA                | 1.00                  |

**AC CHARACTERISTICS FOR 74HCT**

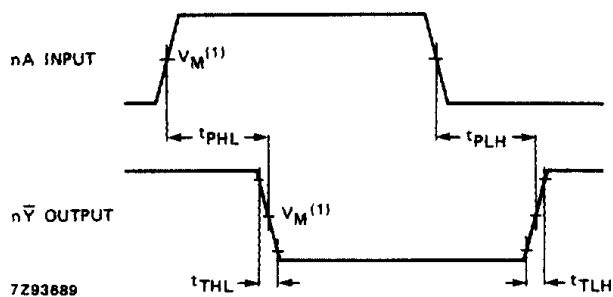
GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

| SYMBOL                              | PARAMETER                                                            | T <sub>amb</sub> (°C) |      |      |            |      |             |      | UNIT | TEST CONDITIONS        |           |
|-------------------------------------|----------------------------------------------------------------------|-----------------------|------|------|------------|------|-------------|------|------|------------------------|-----------|
|                                     |                                                                      | 74HCT                 |      |      |            |      |             |      |      | V <sub>CC</sub><br>(V) | WAVEFORMS |
|                                     |                                                                      | +25                   |      |      | −40 to +85 |      | −40 to +125 |      |      |                        |           |
|                                     |                                                                      | min.                  | typ. | max. | min.       | max. | min.        | max. |      |                        |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>nA to n $\overline{Y}$                          |                       | 13   | 24   |            | 30   |             | 36   | ns   | 4.5                    | Fig.6     |
| t <sub>PZH</sub> / t <sub>PZL</sub> | 3-state output enable time<br>n $\overline{OE}$ to n $\overline{Y}$  |                       | 17   | 35   |            | 44   |             | 53   | ns   | 4.5                    | Fig.7     |
| t <sub>PHZ</sub> / t <sub>PLZ</sub> | 3-state output disable time<br>n $\overline{OE}$ to n $\overline{Y}$ |                       | 20   | 35   |            | 44   |             | 53   | ns   | 4.5                    | Fig.7     |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time                                               |                       | 5    | 12   |            | 15   |             | 18   | ns   | 4.5                    | Fig.6     |

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## AC WAVEFORMS



- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 HCT :  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.6 Waveforms showing the input (nA) to output (nY) propagation delays and the output transition times.



- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 HCT :  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.7 Waveforms showing the 3-state enable and disable times.

## PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".