

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT643

Octal bus transceiver; 3-state;
true/inverting

Product specification
File under Integrated Circuits, IC06

December 1990

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74HC/HCT643

FEATURES

- Octal bidirectional bus interface
- True and inverting 3-state outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT643 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT643 are octal transceivers featuring true and inverting 3-state bus compatible outputs in both send and receive directions.

The "643" features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) for direction control. $\overline{OE}$ controls the outputs so that the buses are effectively isolated.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f = 6\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A _n to B _n ; inverting B _n to A _n ; true	$C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$	7 8	8 11	ns ns
C_I	input capacitance		3.5	3.5	pF
$C_{I/O}$	input/output capacitance		10	10	pF
C_{PD}	power dissipation capacitance per transceiver	notes 1 and 2	42	44	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_I = \text{GND to } V_{CC}$
For HCT the condition is $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

ORDERING INFORMATION

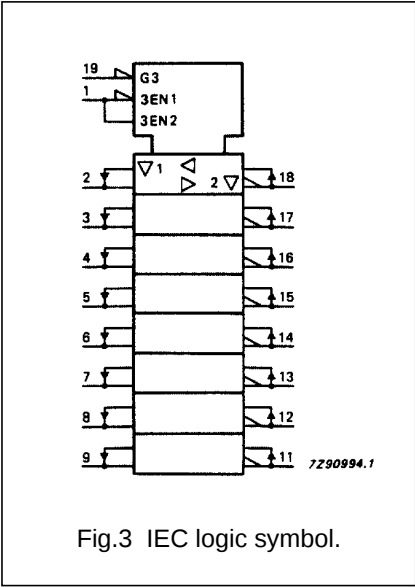
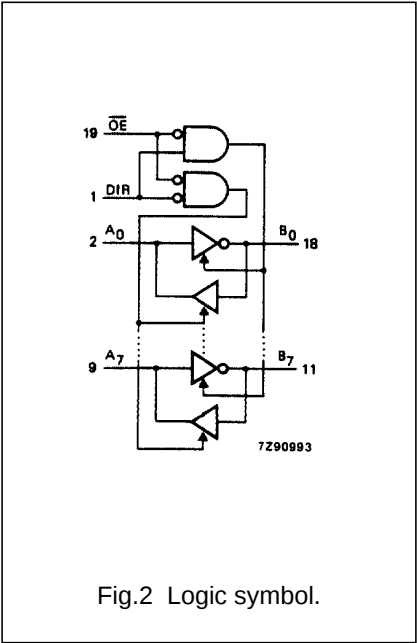
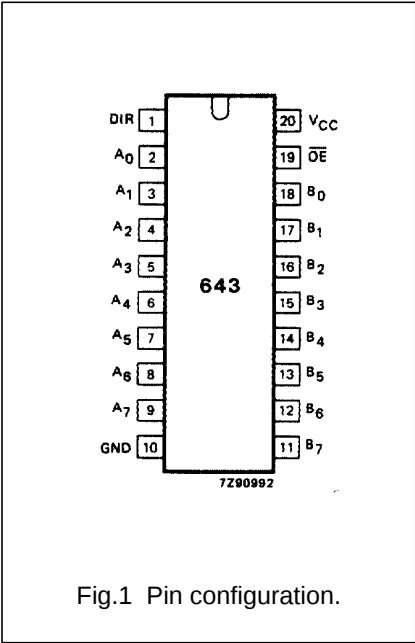
See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

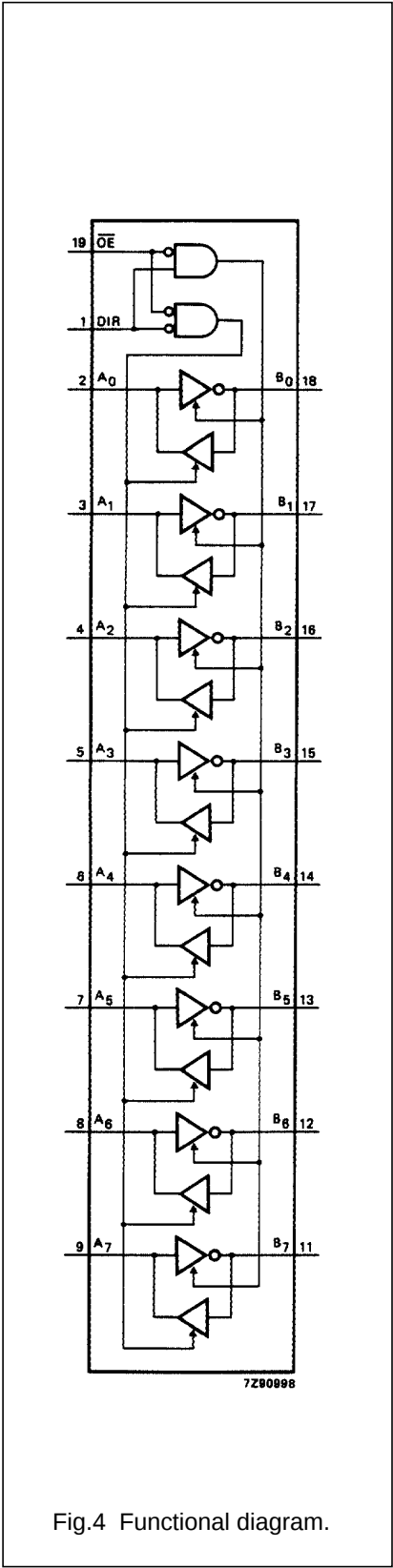
PIN NO.	SYMBOL	NAME AND FUNCTION
1	DIR	direction control
2, 3, 4, 5, 6, 7, 8, 9	A ₀ to A ₇	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B ₀ to B ₇	data inputs/outputs
19	$\overline{\text{OE}}$	output enable input (active LOW)
20	V _{CC}	positive supply voltage



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{\text{OE}}$	DIR	A _n	B _n
L	L	A = B	inputs
L	H	inputs	B = $\overline{\text{A}}$
H	X	Z	Z

- Notes
- H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state



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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay A _n to B _n ; inverting		25 9 7	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig.5
t _{PHL} / t _{PLH}	propagation delay B _n to A _n ; non-inverting (true)		28 10 8	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig.6
t _{PZH} / t _{PZL}	3-state output enable time $\overline{\text{OE}}$, DIR to A _n ; $\overline{\text{OE}}$, DIR to B _n		39 14 11	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.7
t _{PHZ} / t _{PLZ}	3-state output disable time $\overline{\text{OE}}$, DIR to A _n ; $\overline{\text{OE}}$, DIR to B _n		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.7
t _{THL} / t _{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.5 and Fig.6

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A _n	1.50
B _n	0.40
$\overline{OE}$	1.50
DIR	0.90

AC CHARACTERISTICS FOR 74HCT

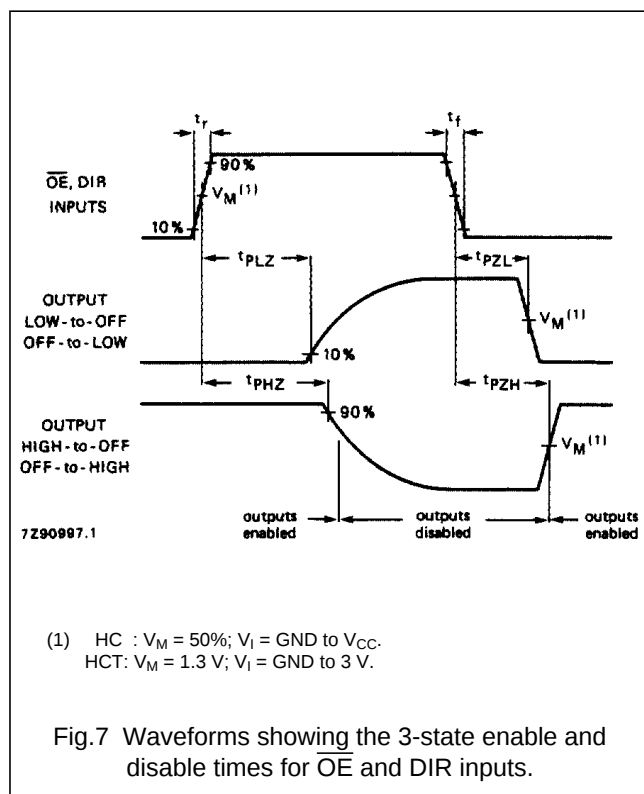
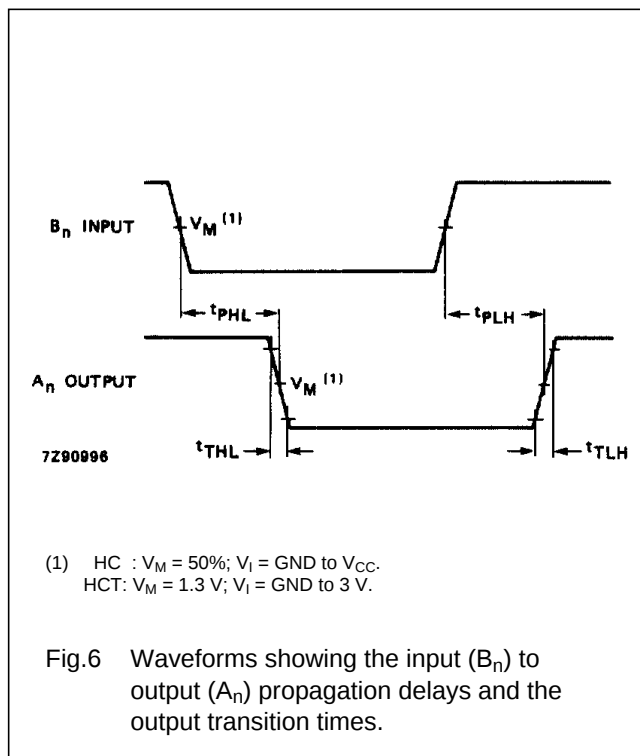
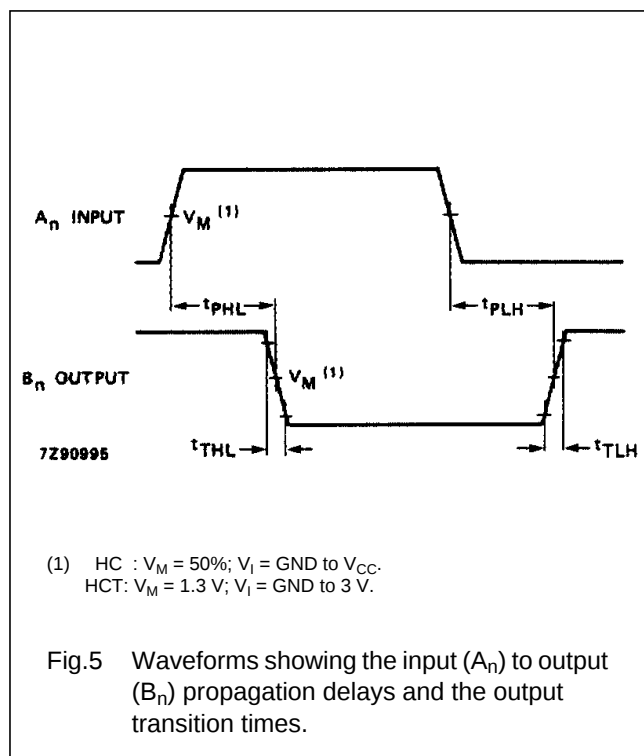
GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay A _n to B _n ; inverting		10	20		25		30	ns	4.5	Fig.5
t _{PHL} / t _{PLH}	propagation delay B _n to A _n ; non-inverting (true)		13	23		29		35	ns	4.5	Fig.6
t _{PZH} / t _{PZL}	3-state output enable time $\overline{OE}$, DIR to A _n ; $\overline{OE}$, DIR to B _n		16	30		38		45	ns	4.5	Fig.7
t _{PHZ} / t _{PLZ}	3-state output disable time $\overline{OE}$, DIR to A _n ; $\overline{OE}$, DIR to B _n		17	30		38		45	ns	4.5	Fig.7
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Fig.5 and Fig.6

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AC WAVEFORMS



PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.