DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT648

Octal bus transceiver/register; 3-state; inverting

Product specification
File under Integrated Circuits, IC06

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Philips Semiconductors

PHILIPS

Octal bus transceiver/register; 3-state; inverting

74HC/HCT648

FEATURES

- Independent register for A and B buses
- Multiplexed real-time and stored data
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT648 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT648 consist of bus transceiver circuits with 3-state inverting outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the "A" or "B" bus will be clocked into the registers as the appropriate clock (CP_{AB} and CP_{BA}) goes to a HIGH logic level. Output enable ($\overline{OE}$) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the "A" or "B" register, or in both. The select source inputs (S_{AB} and S_{BA}) can multiplex stored and real-time (transparent mode) data. The direction (DIR) input determines which bus will receive data when $\overline{OE}$ is active (LOW). In the isolation mode ($\overline{OE}$ = HIGH), "$\overline{A}$" data may be stored in the "B" register and/or "$\overline{B}$" data may be stored in the "A" register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The "648" is functionally identical to the "646", but has inverting data paths.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_n$, $\overline{B}_n$ to $\overline{B}_n$, $\overline{A}_n$	C_L = 15 pF; V_{CC} = 5 V	11	11	ns
f_{max}	maximum clock frequency		75	88	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per channel	notes 1 and 2	30	31	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	CP_{AB}	A to B clock input (LOW-to-HIGH, edge-triggered)
2	S_{AB}	select A to B source input
3	DIR	direction control input
4, 5, 6, 7, 8, 9, 10, 11	$\overline{A}_0$ to $\overline{A}_7$	$\overline{A}$ data inputs/outputs
12	GND	ground (0 V)
20, 19, 18, 17, 16, 15, 14, 13	$\overline{B}_0$ to $\overline{B}_7$	$\overline{B}$ data inputs/outputs
21	$\overline{OE}$	output enable input (active LOW)
22	S_{BA}	select B to A source input
23	CP_{BA}	B to A clock input (LOW-to-HIGH, edge-triggered)
24	V_{CC}	positive supply voltage

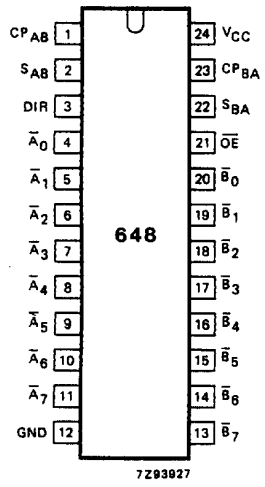


Fig.1 Pin configuration.

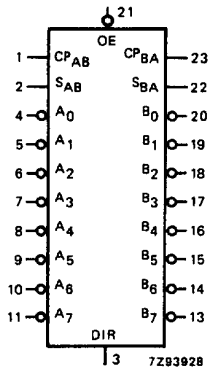


Fig.2 Logic symbol.

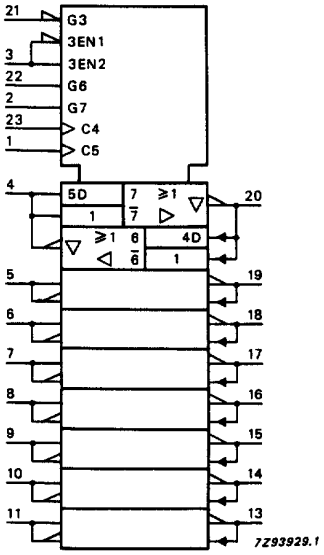


Fig.3 IEC logic symbol.

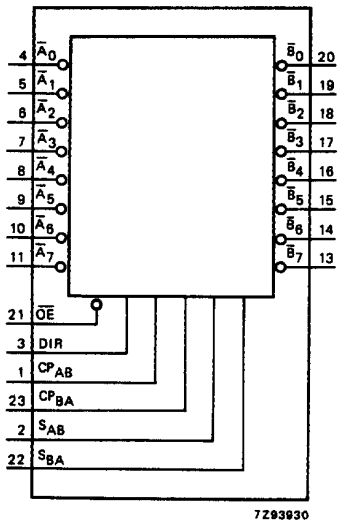


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS (1)						DATA I/O (2)		FUNCTION
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	$\overline{A}_0$ TO $\overline{A}_7$	$\overline{B}_0$ TO $\overline{B}_7$	
H H	X X	H or L ↑	H or L ↑	X X	X X	input	input	isolation store $\overline{A}$ and $\overline{B}$ data
L L	L L	X X	X H or L	X X	L H	output	input	real-time $\overline{B}$ data to A bus stored $\overline{B}$ data to A bus
L L	H H	X H or L	X X	L H	X X	input	output	real-time $\overline{A}$ data to B bus stored $\overline{A}$ data to B bus

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care
   ↑ = LOW-to-HIGH level transition
2. The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

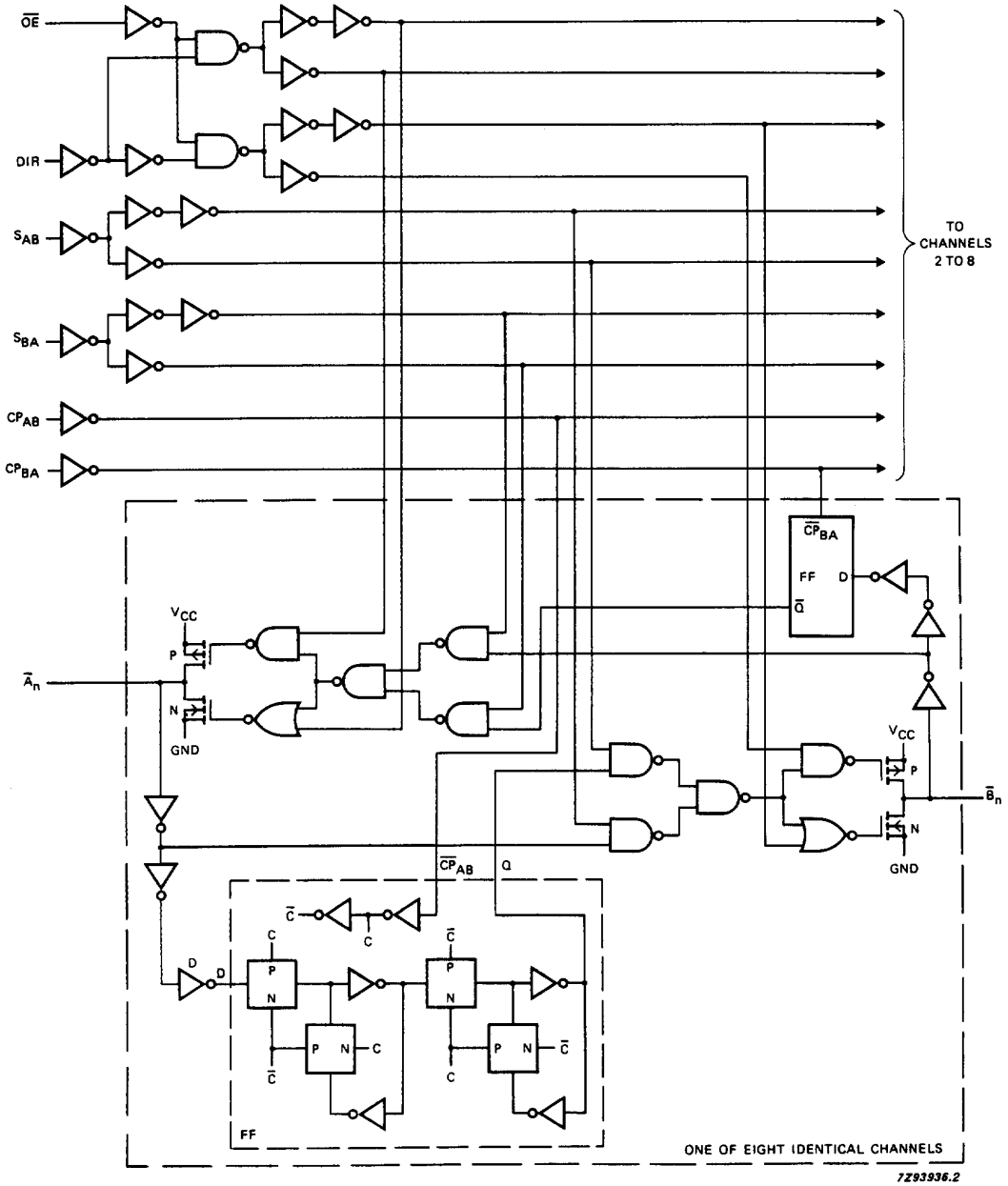


Fig.5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.
Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_n$, $\overline{B}_n$ to $\overline{B}_n$, $\overline{A}_n$		39 14 11	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay CP_{AB}, CP_{BA} to $\overline{B}_n$, $\overline{A}_n$		74 27 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig.7
t_{PHL}/ t_{PLH}	propagation delay S_{AB}, S_{BA} to $\overline{B}_n$, $\overline{A}_n$		55 20 16	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig.8
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{A}_n$, $\overline{B}_n$		52 19 15	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.9
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{A}_n$, $\overline{B}_n$		61 22 18	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.9
t_{PZH}/ t_{PZL}	3-state output enable time DIR to $\overline{A}_n$, $\overline{B}_n$		52 19 15	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.10
t_{PHZ}/ t_{PLZ}	3-state output disable time DIR to $\overline{A}_n$, $\overline{B}_n$		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.10
t_{THL}/ t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.6 and Fig.8
t_W	clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	80 16 14	25 9 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t_{su}	set-up time $\overline{A}_n$, $\overline{B}_n$ to CP_{AB}, CP_{BA}	60 12 10	0 0 0		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.7
t_h	hold time $\overline{A}_n$, $\overline{B}_n$ to CP_{AB}, CP_{BA}	35 7 6	6 2 2		45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig.7
f_{max}	maximum clock pulse frequency	6.0 30 35	22 68 81		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{S}_{AB}$, $\overline{S}_{BA}$	0.60
$\overline{A}_0$ to $\overline{A}_7$; and $\overline{B}_0$ to $\overline{B}_7$;	0.75

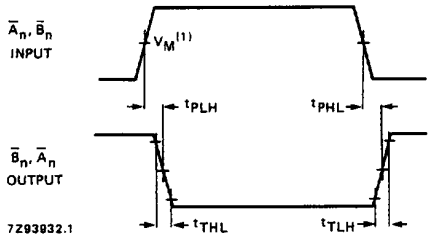
INPUT	UNIT LOAD COEFFICIENT
$\overline{CP}_{AB}$; CP_{BA};	1.50
$\overline{OE}$	1.50
DIR	1.25

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

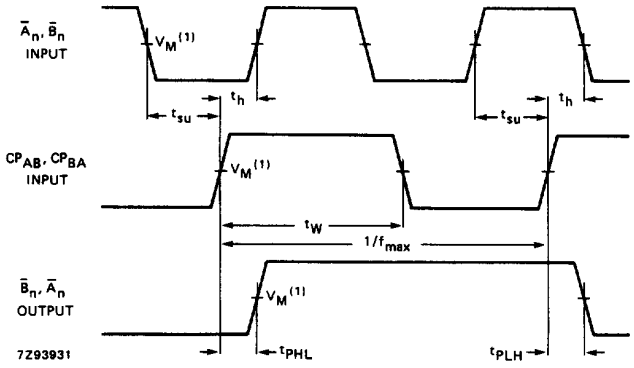
SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_n$, B_n to $\overline{B}_n$, $\overline{A}_n$		14	27		34		41	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay CP_{AB}, CP_{BA} to $\overline{B}_n$, $\overline{A}_n$		25	46		58		69	ns	4.5	Fig.7
t_{PHL}/ t_{PLH}	propagation delay S_{AB}, S_{BA} to $\overline{B}_n$, $\overline{A}_n$		20	38		48		57	ns	4.5	Fig.8
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{A}_n$, $\overline{B}_n$		21	40		50		60	ns	4.5	Fig.9
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{A}_n$, $\overline{B}_n$		20	35		44		53	ns	4.5	Fig.9
t_{PZH}/ t_{PZL}	3-state output enable time DIR to $\overline{A}_n$, $\overline{B}_n$		20	40		50		60	ns	4.5	Fig.10
t_{PHZ}/ t_{PLZ}	3-state output disable time DIR to $\overline{A}_n$, $\overline{B}_n$		21	35		44		53	ns	4.5	Fig.10
t_{THL}/ t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig.6 and Fig.8
t_W	clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	16	7		20		24		ns	4.5	Fig.7
t_{su}	set-up time $\overline{A}_n$, $\overline{B}_n$ to CP_{AB}, CP_{BA}	12	2		15		18		ns	4.5	Fig.7
t_h	hold time $\overline{A}_n$, $\overline{B}_n$ to CP_{AB}, CP_{BA}	5	0		5		5		ns	4.5	Fig.7
f_{max}	maximum clock pulse frequency	30	80		24		20		ns	MHz	Fig.7

AC WAVEFORMS



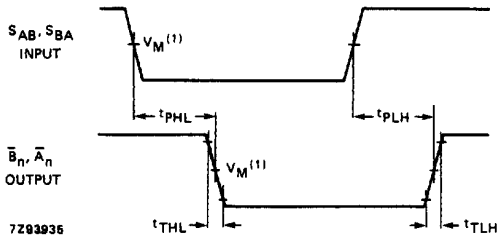
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.6 Waveforms showing the input $\overline{A}_n$, $\overline{B}_n$ to output $\overline{B}_n$, $\overline{A}_n$ propagation delays and the output transition times.



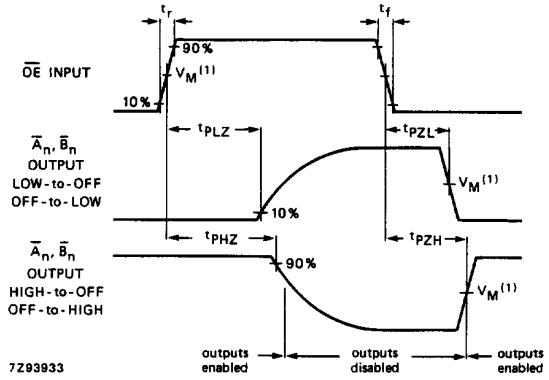
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the $\overline{A}_n$, $\overline{B}_n$ to CP_{AB}, CP_{BA} set-up and hold times, clock CP_{AB}, CP_{BA} pulse width, maximum clock pulse frequency and the CP_{AB}, CP_{BA} to output $\overline{B}_n$, $\overline{A}_n$ propagation delays.



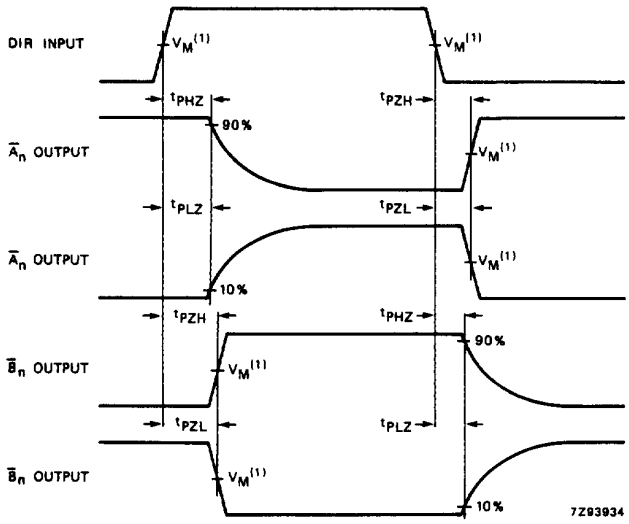
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.8 Waveforms showing the input S_{AB}, S_{BA} to output $\overline{B}_n$, $\overline{A}_n$ propagation delays and output transition times.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.9 Waveforms showing the input $\overline{OE}$ to output $\overline{A}_n$, $\overline{B}_n$ 3-state enable and disable times.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.10 Waveforms showing the input DIR to output $\overline{A}_n$, $\overline{B}_n$ 3-state enable and disable times.

APPLICATION INFORMATION

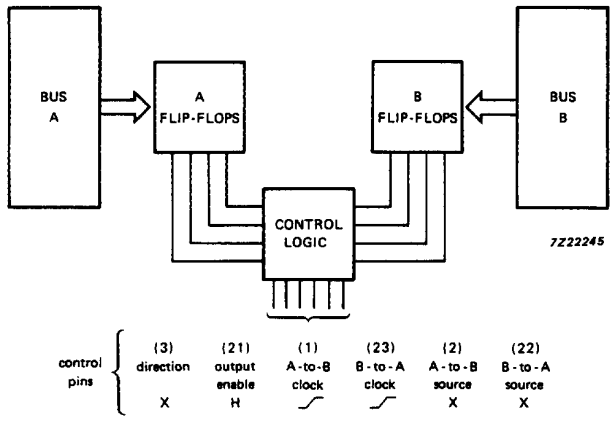


Fig.11 Data storage from A and/or B bus.

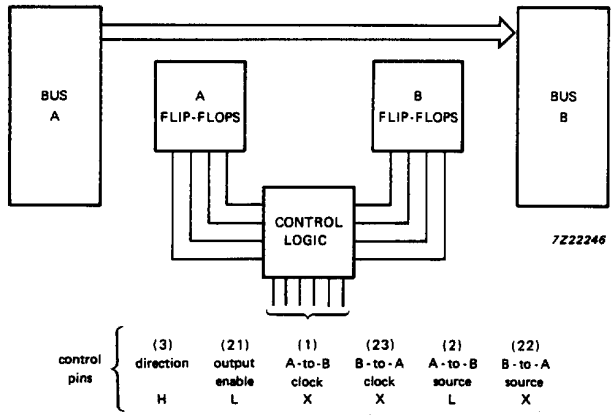


Fig.12 Real-time transfer from bus A to bus B.

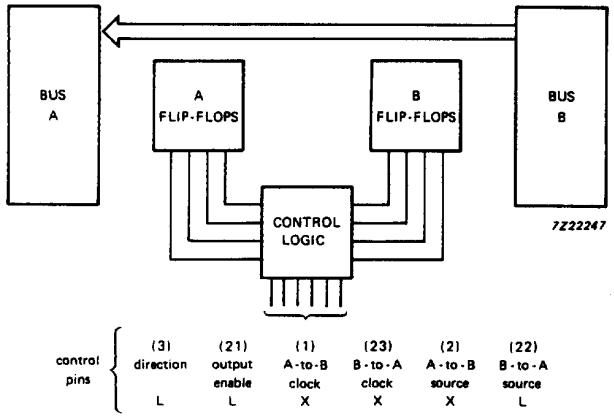


Fig.13 Real-time transfer from bus B to bus A.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.