

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT648

Octal bus transceiver/register;
3-state; inverting

Product specification
File under Integrated Circuits, IC06

December 1990

Octal bus transceiver/register; 3-state; inverting

74HC/HCT648

FEATURES

- Independent register for A and B buses
- Multiplexed real-time and stored data
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT648 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT648 consist of bus transceiver circuits with 3-state inverting outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the "A" or "B"

bus will be clocked into the registers as the appropriate clock (CP_{AB} and CP_{BA}) goes to a HIGH logic level. Output enable ($\overline{OE}$) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the "A" or "B" register, or in both. The select source inputs (S_{AB} and S_{BA}) can multiplex stored and real-time (transparent mode) data. The direction (DIR) input determines which bus will receive data when $\overline{OE}$ is active (LOW). In the isolation mode ($\overline{OE}$ = HIGH), "A" data may be stored in the "B" register and/or "B" data may be stored in the "A" register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The "648" is functionally identical to the "646", but has inverting data paths.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLH}	propagation delay $\overline{A}_n, \overline{B}_n$ to $\overline{B}_n, \overline{A}_n$	C _L = 15 pF; V _{CC} = 5 V	11	11	ns
f _{max}	maximum clock frequency		75	88	MHz
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per channel	notes 1 and 2	30	31	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	CP _{AB}	A to B clock input (LOW-to-HIGH, edge-triggered)
2	S _{AB}	select A to B source input
3	DIR	direction control input
4, 5, 6, 7, 8, 9, 10, 11	$\bar{A}_0$ to $\bar{A}_7$	$\bar{A}$ data inputs/outputs
12	GND	ground (0 V)
20, 19, 18, 17, 16, 15, 14, 13	$\bar{B}_0$ to $\bar{B}_7$	$\bar{B}$ data inputs/outputs
21	$\overline{OE}$	output enable input (active LOW)
22	S _{BA}	select B to A source input
23	CP _{BA}	B to A clock input (LOW-to-HIGH, edge-triggered)
24	V _{CC}	positive supply voltage

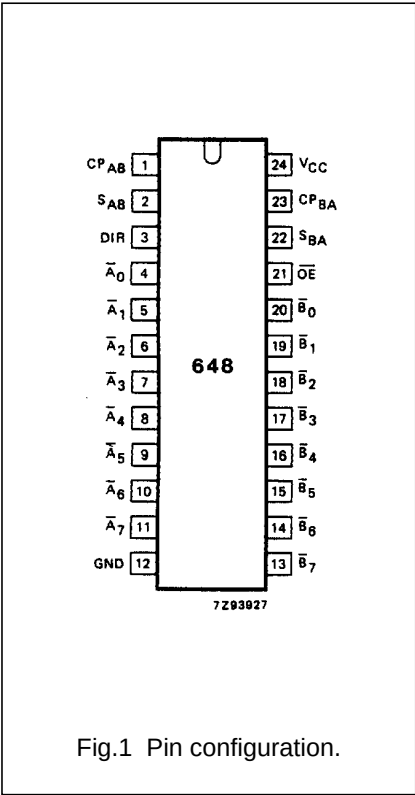


Fig.1 Pin configuration.

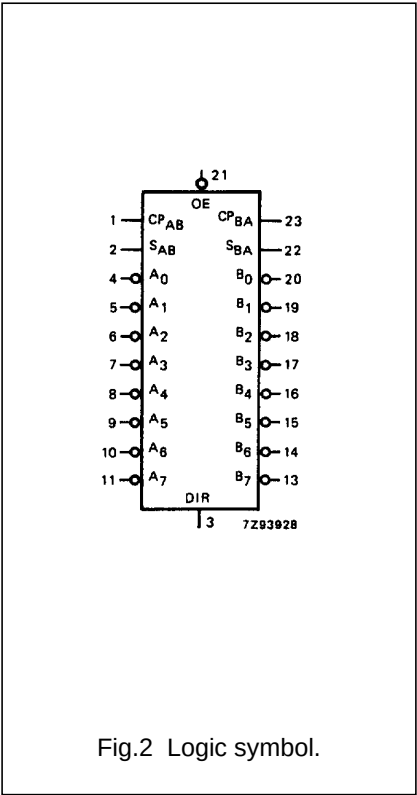


Fig.2 Logic symbol.

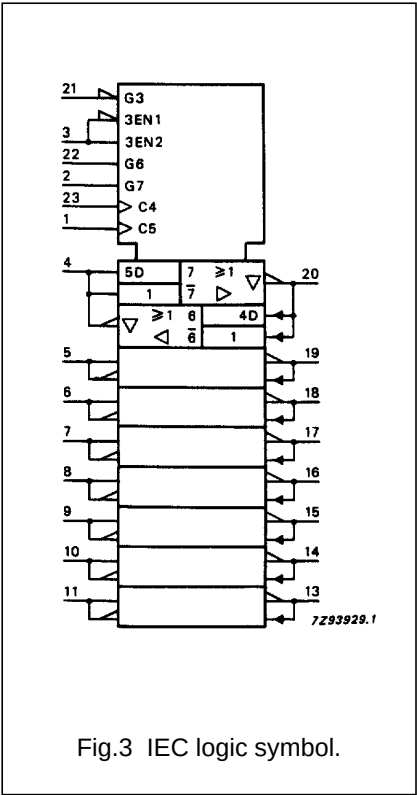
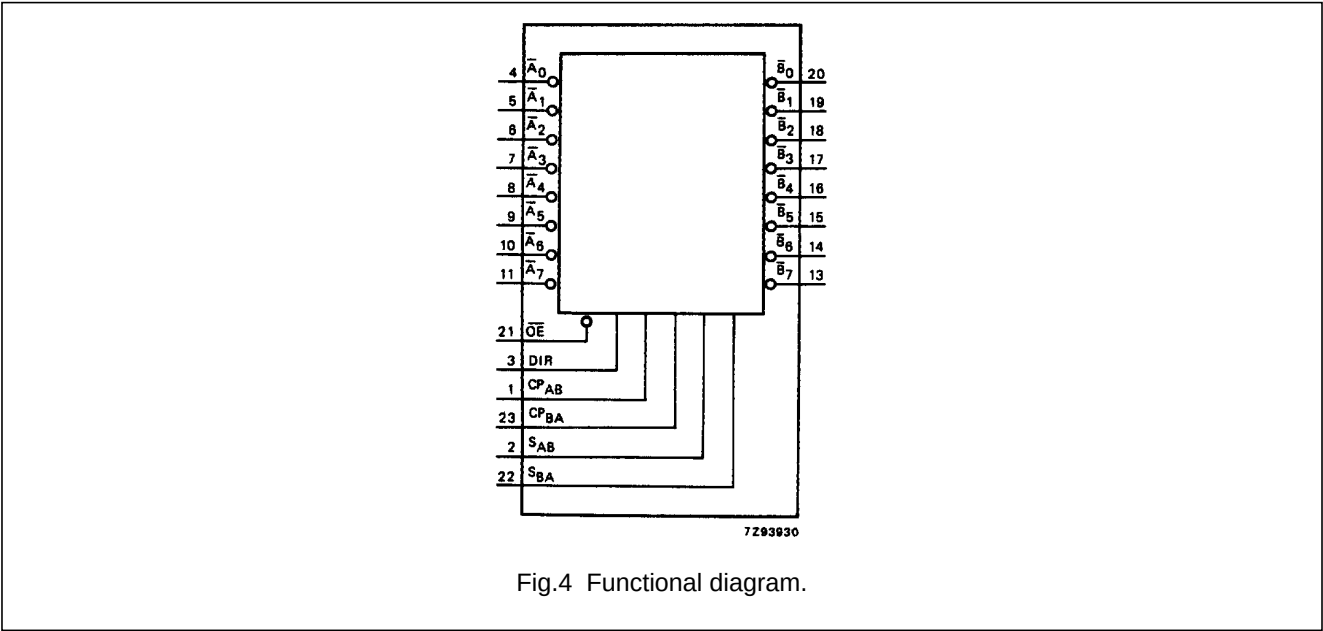


Fig.3 IEC logic symbol.

Octal bus transceiver/register; 3-state;
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FUNCTION TABLE

INPUTS ⁽¹⁾						DATA I/O ⁽²⁾		FUNCTION
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	$\overline{A}_0$ TO $\overline{A}_7$	$\overline{B}_0$ TO $\overline{B}_7$	
H	X	H or L	H or L	X	X	input	input	isolation
H	X	↑	↑	X	X			store $\overline{A}$ and $\overline{B}$ data
L	L	X	X	X	L	output	input	real-time $\overline{B}$ data to A bus
L	L	X	H or L	X	H			stored $\overline{B}$ data to A bus
L	H	X	X	L	X	input	output	real-time $\overline{A}$ data to B bus
L	H	H or L	X	H	X			stored $\overline{A}$ data to B bus

Notes

1. H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level transition
2. The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

Octal bus transceiver/register; 3-state;
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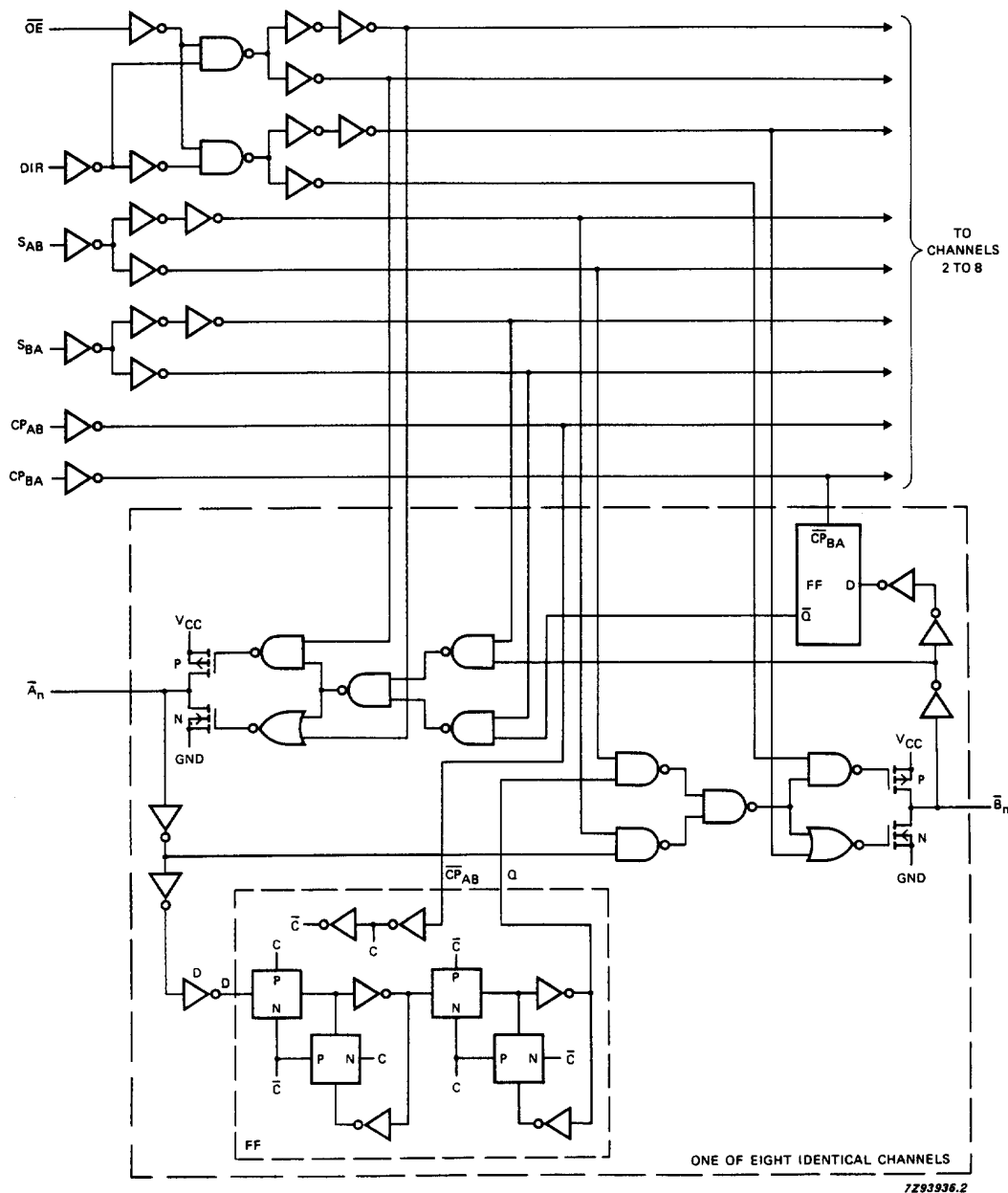


Fig.5 Logic diagram.

Octal bus transceiver/register; 3-state; inverting

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay A _n , B _n to B _n , A _n		39 14 11	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig.6
t _{PHL} / t _{PLH}	propagation delay CP _{AB} , CP _{BA} to B _n , A _n		74 27 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig.7
t _{PHL} / t _{PLH}	propagation delay S _{AB} , S _{BA} to B _n , A _n		55 20 16	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig.8
t _{PZH} / t _{PZL}	3-state output enable time OE to A _n , B _n		52 19 15	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.9
t _{PHZ} / t _{PLZ}	3-state output disable time OE to A _n , B _n		61 22 18	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.9
t _{PZH} / t _{PZL}	3-state output enable time DIR to A _n , B _n		52 19 15	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.10
t _{PHZ} / t _{PLZ}	3-state output disable time DIR to A _n , B _n		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.10
t _{THL} / t _{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.6 and Fig.8
t _W	clock pulse width HIGH or LOW CP _{AB} or CP _{BA}	80 16 14	25 9 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t _{su}	set-up time A _n , B _n to CP _{AB} , CP _{BA}	60 12 10	0 0 0		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.7
t _h	hold time A _n , B _n to CP _{AB} , CP _{BA}	35 7 6	6 2 2		45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig.7
f _{max}	maximum clock pulse frequency	6.0 30 35	22 68 81		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.7

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74HC/HCT648**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{S}_{AB}$, $\overline{S}_{BA}$	0.60
$\overline{A}_0$ to $\overline{A}_7$; and $\overline{B}_0$ to $\overline{B}_7$;	0.75

INPUT	UNIT LOAD COEFFICIENT
$\overline{CP}_{AB}$; $\overline{CP}_{BA}$;	1.50
$\overline{OE}$	1.50
$\overline{DIR}$	1.25

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AC CHARACTERISTICS FOR 74HCTGND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay A _n , B _n to B _n , A _n		14	27		34		41	ns	4.5	Fig.6
t _{PHL} / t _{PLH}	propagation delay CP _{AB} , CP _{BA} to B _n , A _n		25	46		58		69	ns	4.5	Fig.7
t _{PHL} / t _{PLH}	propagation delay S _{AB} , S _{BA} to B _n , A _n		20	38		48		57	ns	4.5	Fig.8
t _{PZH} / t _{PZL}	3-state output enable time OE to A _n , B _n		21	40		50		60	ns	4.5	Fig.9
t _{PHZ} / t _{PLZ}	3-state output disable time OE to A _n , B _n		20	35		44		53	ns	4.5	Fig.9
t _{PZH} / t _{PZL}	3-state output enable time DIR to A _n , B _n		20	40		50		60	ns	4.5	Fig.10
t _{PHZ} / t _{PLZ}	3-state output disable time DIR to A _n , B _n		21	35		44		53	ns	4.5	Fig.10
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Fig.6 and Fig.8
t _W	clock pulse width HIGH or LOW CP _{AB} or CP _{BA}	16	7		20		24		ns	4.5	Fig.7
t _{su}	set-up time A _n , B _n to CP _{AB} , CP _{BA}	12	2		15		18		ns	4.5	Fig.7
t _h	hold time A _n , B _n to CP _{AB} , CP _{BA}	5	0		5		5		ns	4.5	Fig.7
f _{max}	maximum clock pulse frequency	30	80		24		20		ns	MHz	Fig.7

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AC WAVEFORMS

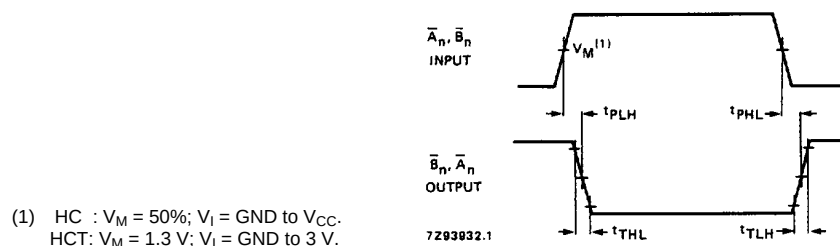


Fig.6 Waveforms showing the input $\bar{A}_n, \bar{B}_n$ to output $\bar{B}_n, \bar{A}_n$ propagation delays and the output transition times.

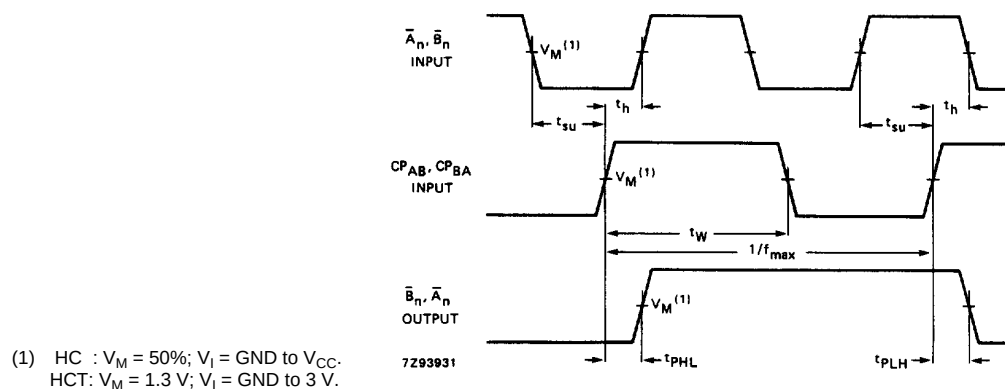


Fig.7 Waveforms showing the $\bar{A}_n, \bar{B}_n$ to CP_{AB}, CP_{BA} set-up and hold times, clock CP_{AB}, CP_{BA} pulse width, maximum clock pulse frequency and the CP_{AB}, CP_{BA} to output $\bar{B}_n, \bar{A}_n$ propagation delays.

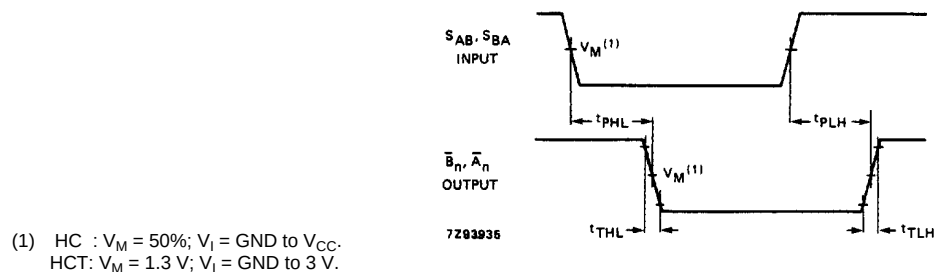


Fig.8 Waveforms showing the input S_{AB}, S_{BA} to output $\bar{B}_n, \bar{A}_n$ propagation delays and output transition times.

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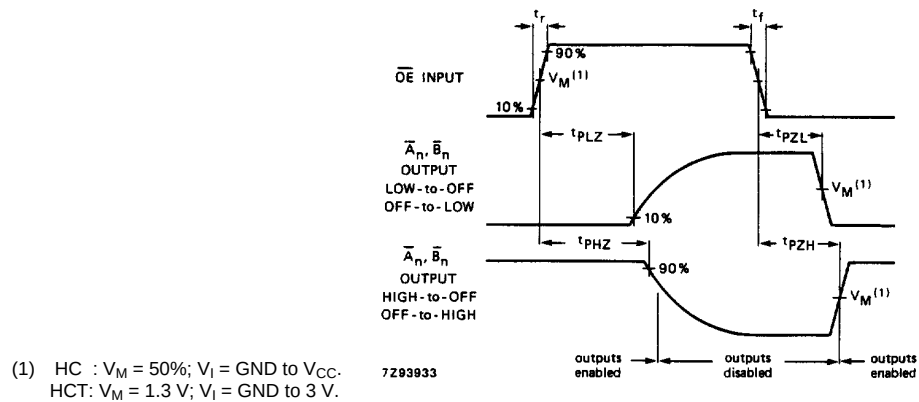


Fig.9 Waveforms showing the input $\overline{\text{OE}}$ to output $\overline{\text{A}}_n$, $\overline{\text{B}}_n$ 3-state enable and disable times.

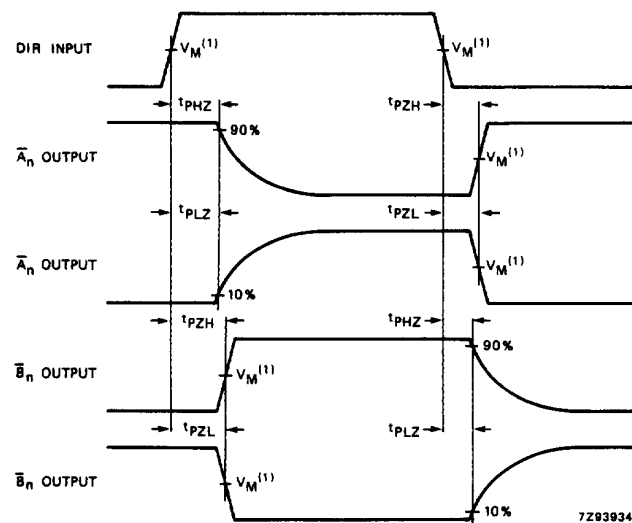
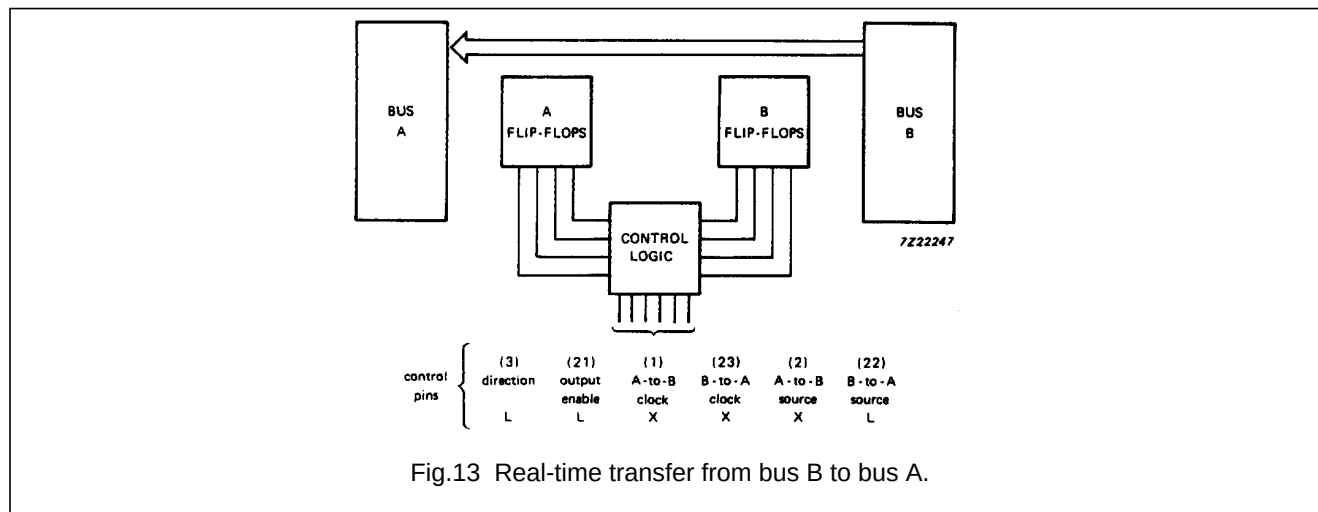
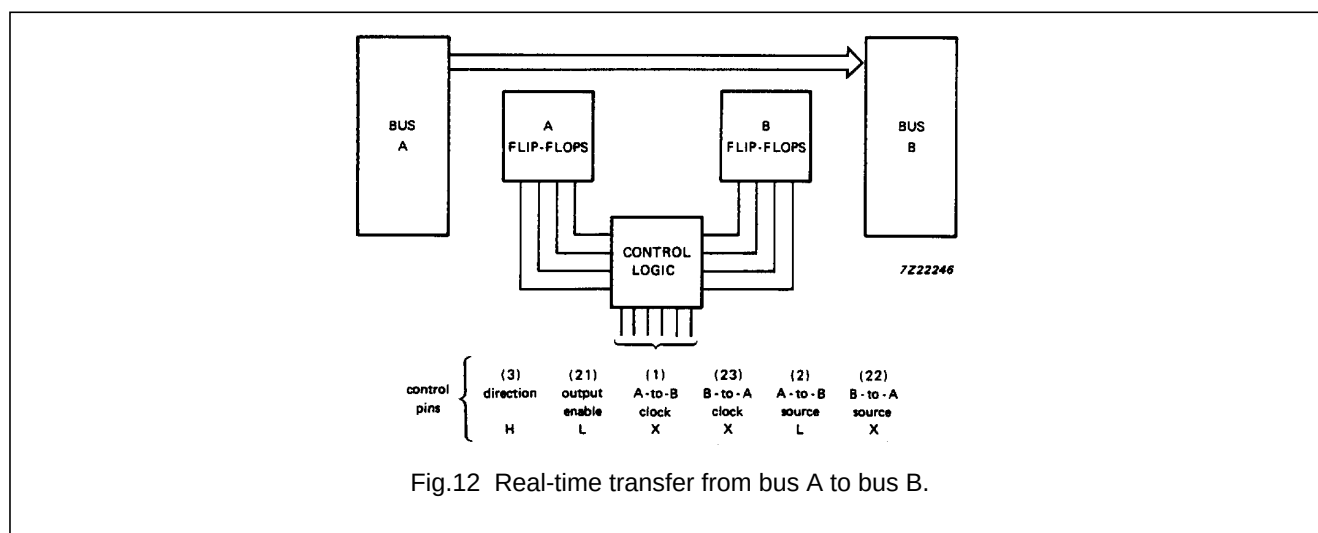
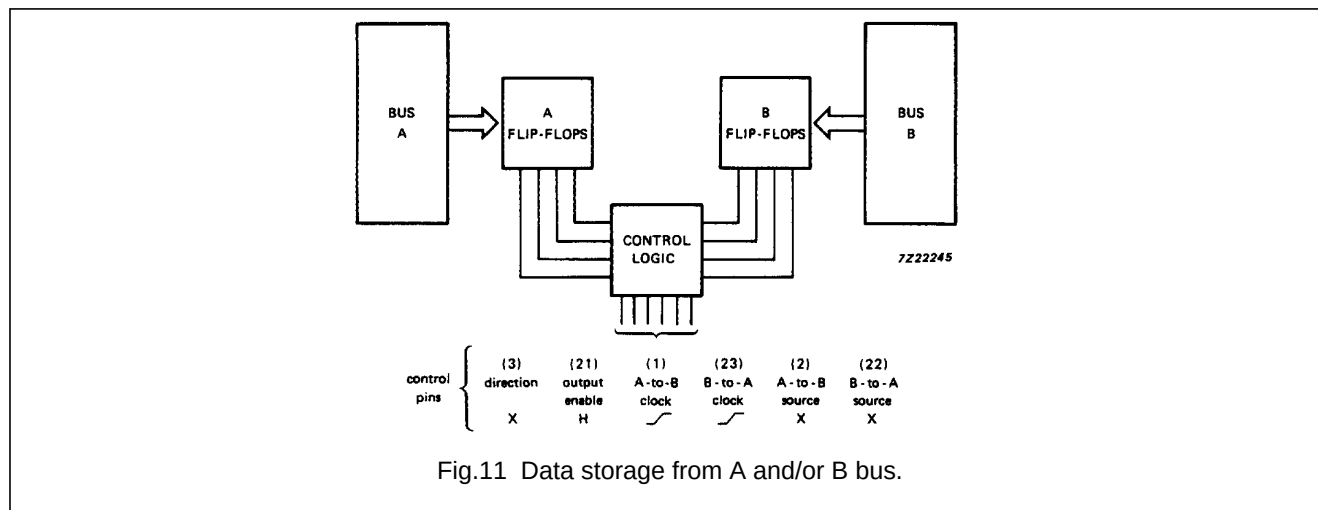


Fig.10 Waveforms showing the input DIR to output $\bar{A}_n$, $\bar{B}_n$ 3-state enable and disable times.

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APPLICATION INFORMATION



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PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.