

DATA SHEET

74LVC1G02

Single 2-input NOR gate

Product specification
Supersedes data of 2001 Apr 11

2002 May 15

Single 2-input NOR gate

74LVC1G02

FEATURES

- Wide supply voltage range from 1.65 to 5.5 V
- High noise immunity
- Complies with JEDEC standard:
 - JESD8-7 (1.65 to 1.95 V)
 - JESD8-5 (2.3 to 2.7 V)
 - JESD8B/JESD36 (2.7 to 3.6 V).
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low power consumption
- Latch-up performance ≤ 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from -40 to $+125$ °C.

DESCRIPTION

The 74LVC1G02 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Input can be driven from either 3.3 or 5 V devices. These features allow the use of these devices in a mixed 3.3 and 5 V environment.

Schmitt trigger action at all inputs makes the circuit tolerant for slower input rise and fall time.

This device is fully specified for partial power-down applications using I_{off} . The I_{off} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74LVC1G02 provides the single 2-input NOR function.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay inputs A, B to output Y	$V_{CC} = 1.8$ V; $C_L = 30$ pF; $R_L = 1$ k Ω	3.2	ns
		$V_{CC} = 2.5$ V; $C_L = 30$ pF; $R_L = 500$ Ω	2.2	ns
		$V_{CC} = 2.7$ V; $C_L = 50$ pF; $R_L = 500$ Ω	2.5	ns
		$V_{CC} = 3.3$ V; $C_L = 50$ pF; $R_L = 500$ Ω	2.1	ns
		$V_{CC} = 5.0$ V; $C_L = 50$ pF; $R_L = 500$ Ω	1.7	ns
C_I	input capacitance		5	pF
C_{PD}	power dissipation capacitance per buffer	$V_{CC} = 3.3$ V; notes 1 and 2	14	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts.

2. The condition is $V_I = \text{GND}$ to V_{CC} .

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FUNCTION TABLE

See note 1.

INPUT		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

Note

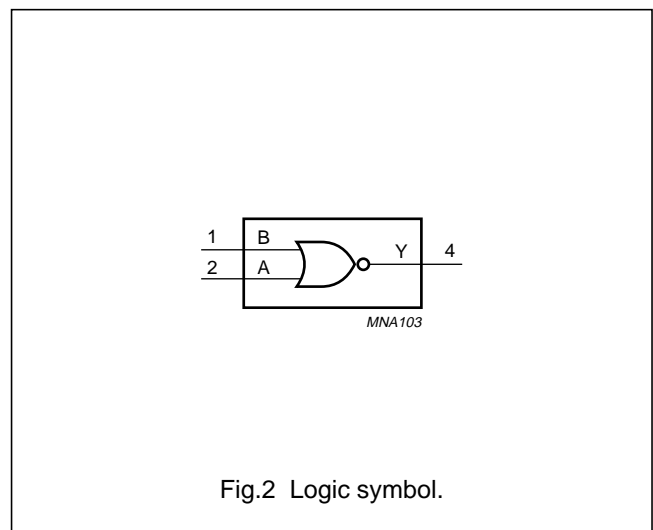
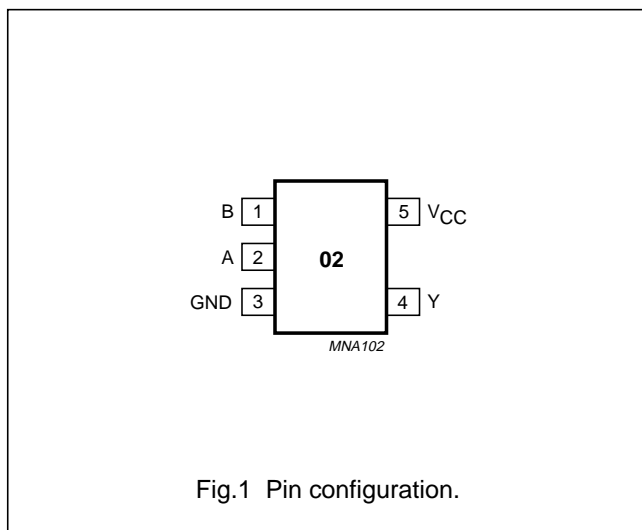
- H = HIGH voltage level;
L = LOW voltage level.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74LVC1G02GW	-40 to +125 °C	5	SC-88A	plastic	SOT353	VB
74LVC1G02GV	-40 to +125 °C	5	SC-74A	plastic	SOT753	V02

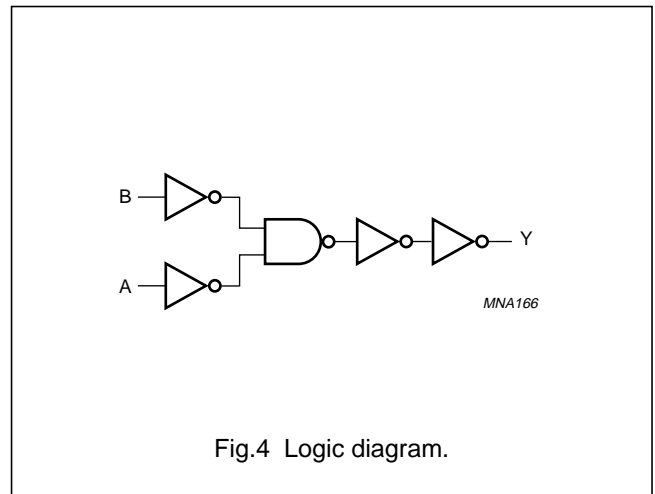
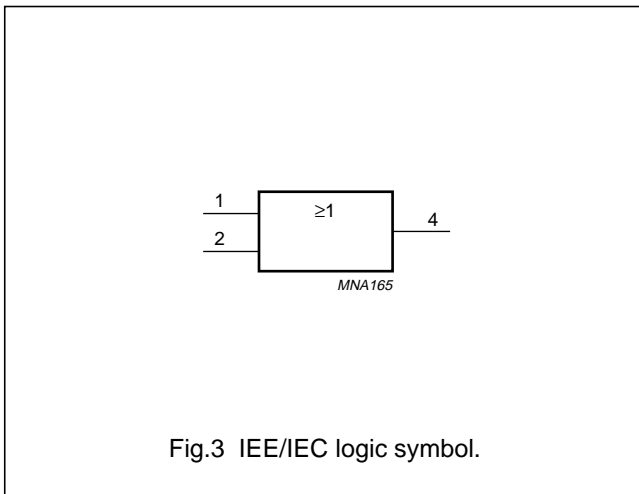
PINNING

PIN	SYMBOL	DESCRIPTION
1	B	data input B
2	A	data input A
3	GND	ground (0 V)
4	Y	data output Y
5	V _{CC}	supply voltage



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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CC}	supply voltage		1.65	5.5	V
V _I	input voltage		0	5.5	V
V _O	output voltage	active mode	0	V _{CC}	V
		V _{CC} = 0 V; Power-down mode	0	5.5	V
T _{amb}	operating ambient temperature		-40	+125	°C
t _r , t _f	input rise and fall times	V _{CC} = 1.65 to 2.7 V	0	20	ns/V
		V _{CC} = 2.7 to 5.5 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input diode current	V _I < 0	-	-50	mA
V _I	input voltage	note 1	-0.5	+6.5	V
I _{OK}	output diode current	V _O > V _{CC} or V _O < 0	-	±50	mA
V _O	output voltage	active mode; notes 1 and 2	-0.5	V _{CC} + 0.5	V
		Power-down mode; notes 1 and 2	-0.5	+6.5	V
I _O	output diode current	V _O = 0 to V _{CC}	-	±50	mA
I _{CC} , I _{GND}	V _{CC} or GND current		-	±100	mA
T _{stg}	storage temperature		-65	+150	°C
P _D	power dissipation per package	for temperature range from -40 to +125 °C	-	250	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. When V_{CC} = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.

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DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)					UNIT	
		OTHER	V_{CC} (V)	-40 to +85			-40 to +125			
				MIN.	TYP. ⁽¹⁾	MAX.	MIN.	MAX.		
V_{IH}	HIGH-level input voltage		1.65 to 1.95	$0.65 \times V_{CC}$	–	–	–	$0.65 \times V_{CC}$	–	V
			2.3 to 2.7	1.7	–	–	–	1.7	–	V
			2.7 to 3.6	2.0	–	–	–	2.0	–	V
			4.5 to 5.5	$0.7 \times V_{CC}$	–	–	–	$0.7 \times V_{CC}$	–	V
V_{IL}	LOW-level input voltage		1.65 to 1.95	–	–	–	$0.35 \times V_{CC}$	–	$0.35 \times V_{CC}$	V
			2.3 to 2.7	–	–	–	0.7	–	0.7	V
			2.7 to 3.6	–	–	–	0.8	–	0.8	V
			4.5 to 5.5	–	–	–	$0.3 \times V_{CC}$	–	$0.3 \times V_{CC}$	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}	1.65 to 5.5	–	–	–	–	–	–	V
		$I_O = 100 \mu A$		–	–	–	0.1	–	0.1	V
		$I_O = 4 \text{ mA}$		–	–	–	0.45	–	0.70	V
		$I_O = 8 \text{ mA}$		–	–	–	0.3	–	0.45	V
		$I_O = 12 \text{ mA}$		–	–	–	0.4	–	0.60	V
		$I_O = 24 \text{ mA}$		–	–	–	0.55	–	0.80	V
$I_O = 32 \text{ mA}$	–	–	–	0.55	–	0.80	V			
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}	1.65 to 5.5	$V_{CC} - 0.1$	–	–	–	$V_{CC} - 0.1$	–	V
		$I_O = -100 \mu A$		–	–	–	0.95	–	V	
		$I_O = -4 \text{ mA}$		–	–	–	1.7	–	V	
		$I_O = -8 \text{ mA}$		–	–	–	1.9	–	V	
		$I_O = -12 \text{ mA}$		–	–	–	2.0	–	V	
		$I_O = -24 \text{ mA}$		–	–	–	3.4	–	V	
$I_O = -32 \text{ mA}$	–	–	–	3.8	–	V				
I_I	input leakage current	$V_I = 5.5 \text{ V}$ or GND	5.5	–	± 0.1	± 5	–	± 100	μA	

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SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)					UNIT
		OTHER	V_{CC} (V)	-40 to +85			-40 to +125		
				MIN.	TYP. ⁽¹⁾	MAX.	MIN.	MAX.	
I_{off}	power OFF leakage current	V_I or $V_O = 5.5$ V	0	–	± 0.1	± 10	–	± 200	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$	5.5	–	0.1	10	–	200	μA
ΔI_{CC}	additional quiescent supply current per pin	$V_I = V_{CC} - 0.6$ V; $I_O = 0$	2.3 to 5.5	–	5	500	–	5000	μA

Note

1. All typical values are measured at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C.

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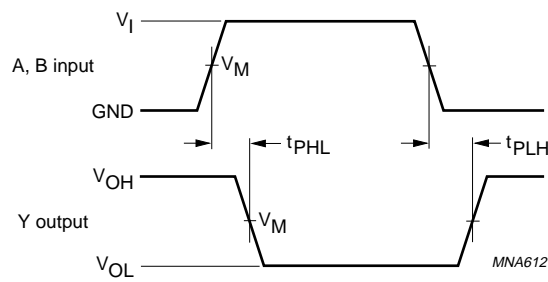
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AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.0$ ns.

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)					UNIT
		WAVEFORMS	V_{CC} (V)	-40 to +85			-40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PHL}/t_{PLH}	propagation delay A, B to Y	see Figs 5 and 6	1.65 to 1.95	1.0	3.2	8.0	1.0	10.5	ns
			2.3 to 2.7	0.5	2.2	5.5	0.5	7.0	ns
			2.7	0.5	2.5	5.5	0.5	7.0	ns
			3.0 to 3.6	0.5	2.1	4.5	0.5	6.0	ns
			4.5 to 5.5	0.5	1.7	4.0	0.5	5.5	ns

AC WAVEFORMS



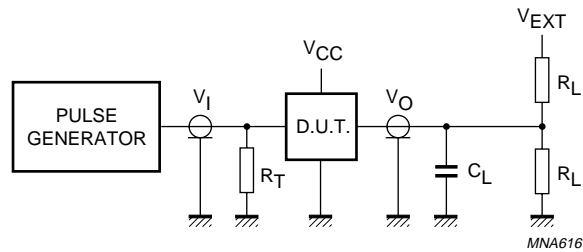
V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.65 to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.3 to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 to 5.5 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.5 A, B to Y propagation delay times.

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V _{CC}	V _I	C _L	R _L	V _{EXT}		
				t _{PLH} /t _{PHL}	t _{PZH} /t _{PHZ}	t _{PZL} /t _{PLZ}
1.65 to 1.95 V	V _{CC}	30 pF	1 kΩ	open	GND	2 × V _{CC}
2.3 to 2.7 V	V _{CC}	30 pF	500 Ω	open	GND	2 × V _{CC}
2.7 V	2.7 V	50 pF	500 Ω	open	GND	6 V
3.0 to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	6 V
4.5 to 5.5 V	V _{CC}	50 pF	500 Ω	open	GND	2 × V _{CC}

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.6 Load circuitry for switching times.

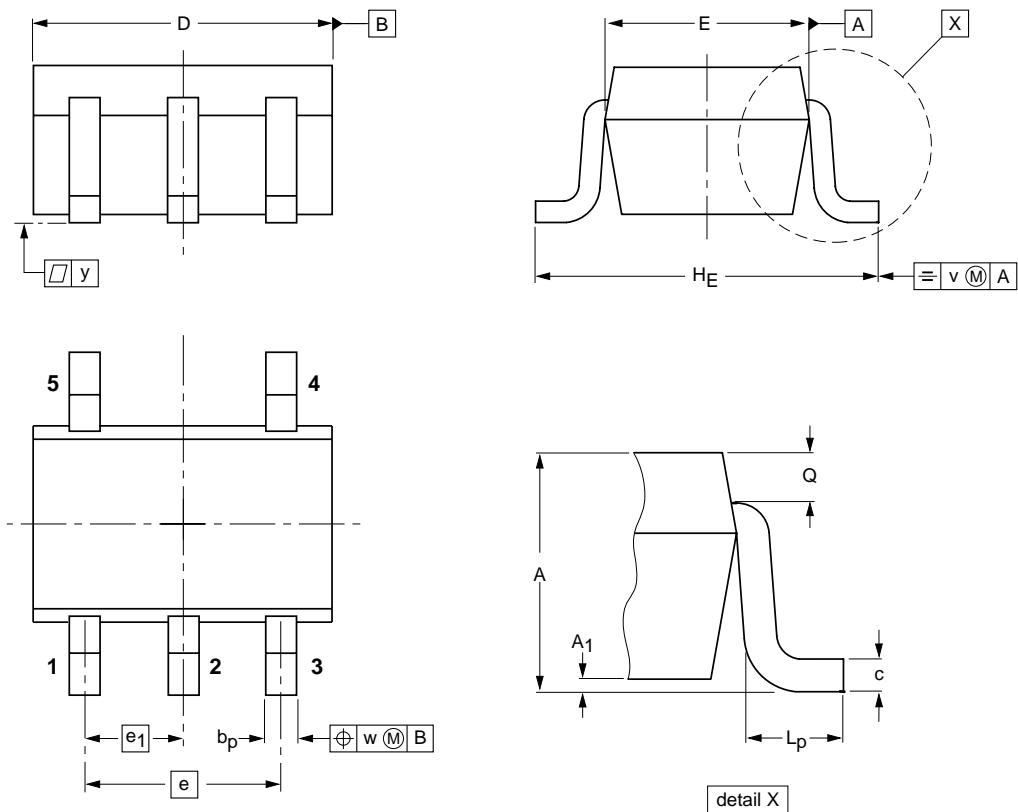
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PACKAGE OUTLINES

Plastic surface mounted package; 5 leads

SOT353



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	c	D	E ⁽²⁾	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

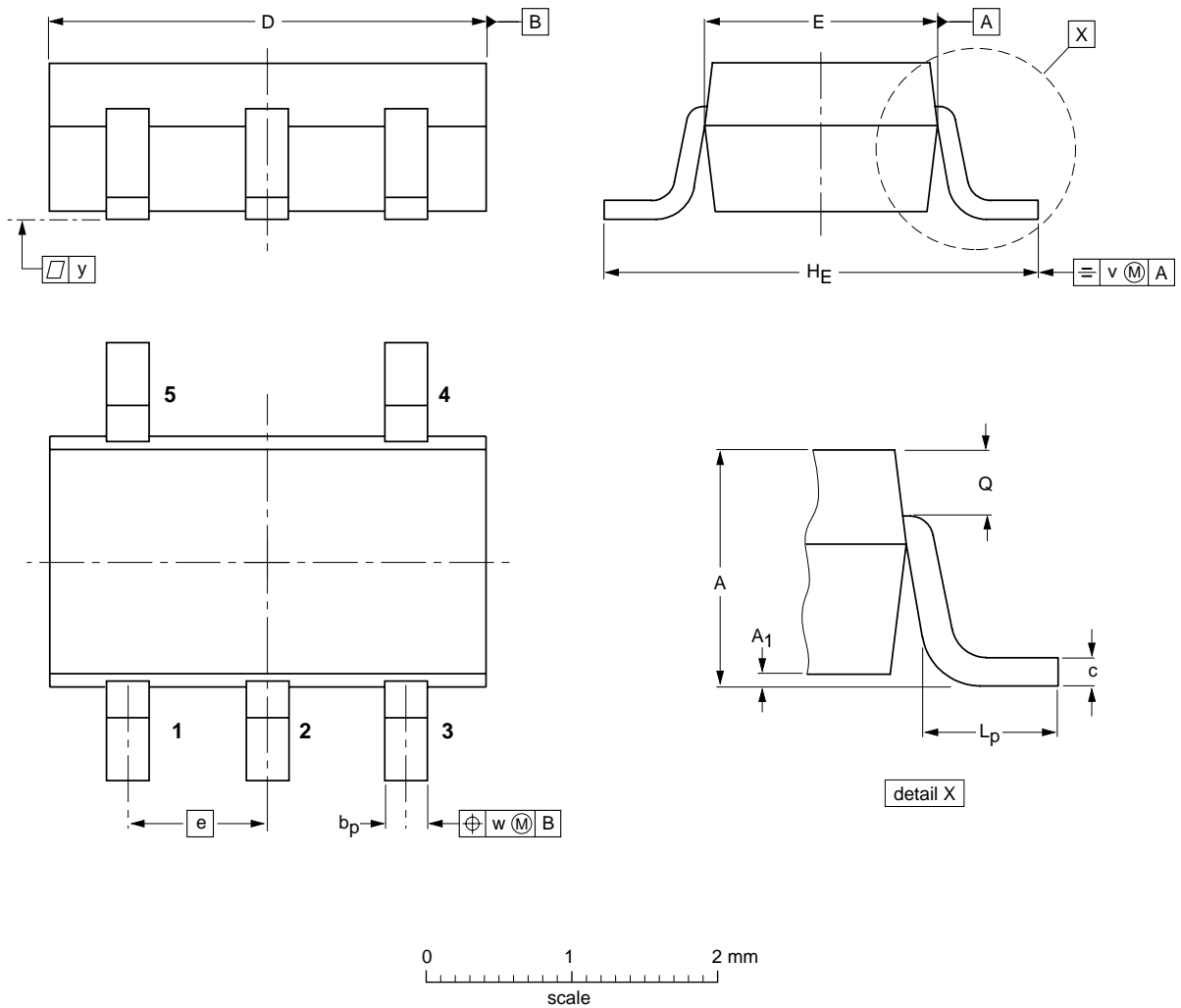
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT353			SC-88A			97-02-28

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Plastic surface mounted package; 5 leads

SOT753



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b _p	c	D	E	e	H _E	L _p	Q	v	w	y
mm	1.1 0.9	0.100 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT753			SC-74A			02-04-16

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SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW ⁽¹⁾
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable ⁽²⁾	suitable
PLCC ⁽³⁾ , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ⁽³⁾⁽⁴⁾	suitable
SSOP, TSSOP, VSO	not recommended ⁽⁵⁾	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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DATA SHEET STATUS

DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

DEFINITIONS

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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NOTES

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NOTES

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