# DATA SHEET


## PCA9544

4-channel $I^2C$ multiplexer with interrupt logic

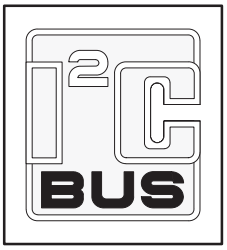
Product data
Supersedes data of 2002 Feb 20

2002 Jul 26

Philips
Semiconductors


PHILIPS

# 4-channel I²C multiplexer with interrupt logic PCA9544




## FEATURES

- 1-of-4 bi-directional translating multiplexer
- I²C interface logic; compatible with SMBus
- 4 Active Low Interrupt Inputs
- Active Low Interrupt Output
- 3 address pins allowing up to 8 devices on the I²C bus
- Channel selection via I²C bus
- Power up with all multiplexer channels deselected
- Low $Rds_{ON}$ switches
- Allows voltage level translation between 1.8 V, 2.5 V, 3.3 V and 5 V buses
- No glitch on power-up
- Supports hot insertion
- Low stand-by current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 5 V tolerant Inputs
- 0 to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 150 V MM per JESD22-A115 and 1000 V per JESD22-C101
- Latchup testing is done to JESDEC Standard JESD78 which exceeds 100 mA
- Three packages offered: SO20, TSSOP20, and HVQFN20

## DESCRIPTION

The PCA9544 is a 1-of-4 bi-directional translating multiplexer, controlled via the I²C bus. The SCL/SDA upstream pair fans out to four SCx/SDx downstream pairs, or channels. Only one SCx/SDx channel is selected at a time, determined by the contents of the programmable control register. Four interrupt inputs, $\overline{INT0}$ to $\overline{INT3}$, one for each of the SCx/SDx downstream pairs, are provided. One interrupt output, $\overline{INT}$, which acts as an AND of the four interrupt inputs, is provided.

A power-on reset function puts the registers in their default state and initializes the I²C state machine with no channels selected.

The pass gates of the multiplexer are constructed such that the $V_{DD}$ pin can be used to limit the maximum high voltage which will be passed by the PCA9544. This allows the use of different bus voltages on each SCx/SDx pair, so that 1.8 V, 2.5 V or 3.3 V parts can communicate with 5 V parts without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5 V tolerant.

## ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | ORDER CODE | TOPSIDE MARK | DRAWING NUMBER |
|---|---|---|---|---|
| 20-Pin Plastic SO | –40 to +85 °C | PCA9544D | PCA9544D | SOT163-1 |
| 20-Pin Plastic TSSOP | –40 to +85 °C | PCA9544PW | PCA9544 | SOT360-1 |
| 20-Pin Plastic HVQFN | –40 to +85 °C | PCA9544BS | 9544 | SOT662-1 |

Standard packing quantities and other packaging data are available at www.philipslogic.com/packaging.

## PIN CONFIGURATION — SO, TSSOP

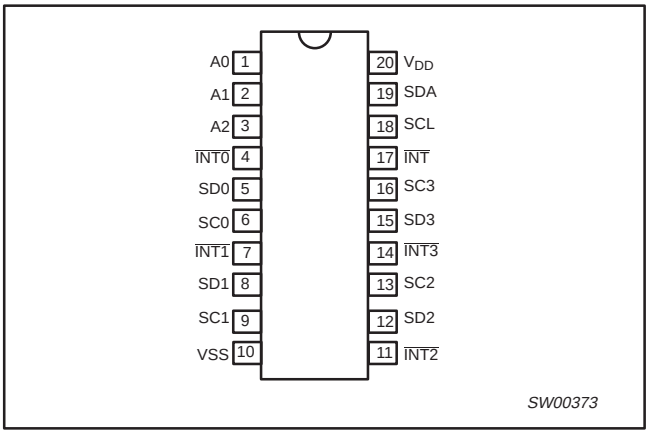



**Figure 1. Pin configuration — SO, TSSOP**

## PIN CONFIGURATION — HVQFN

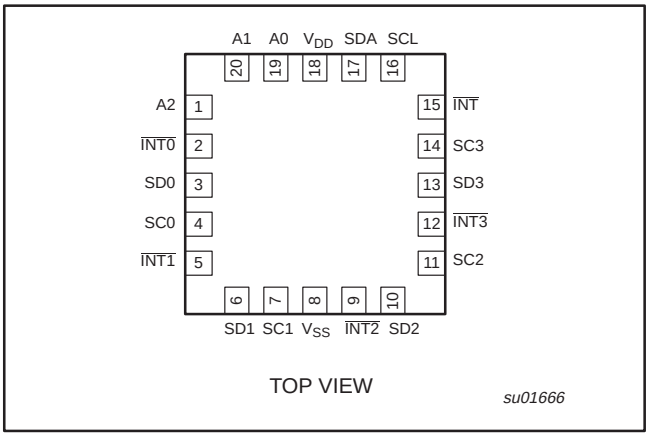



**Figure 2. Pin configuration — HVQFN**

## PIN DESCRIPTION

| SO, TSSOP PIN NUMBER | HVQFN PIN NUMBER | SYMBOL | FUNCTION |
|---|---|---|---|
| 1 | 19 | A0 | Address input 0 |
| 2 | 20 | A1 | Address input 1 |
| 3 | 1 | A2 | Address input 2 |
| 4 | 2 | $\overline{INT0}$ | Active LOW interrupt input 0 |
| 5 | 3 | SD0 | Serial data 0 |
| 6 | 4 | SC0 | Serial clock 0 |
| 7 | 5 | $\overline{INT1}$ | Active LOW interrupt input 1 |
| 8 | 6 | SD1 | Serial data 1 |
| 9 | 7 | SC1 | Serial clock 1 |
| 10 | 8 | $V_{SS}$ | Supply ground |
| 11 | 9 | $\overline{INT2}$ | Active LOW interrupt input 2 |
| 12 | 10 | SD2 | Serial data 2 |
| 13 | 11 | SC2 | Serial clock 2 |
| 14 | 12 | $\overline{INT3}$ | Active LOW interrupt input 3 |
| 15 | 13 | SD3 | Serial data 3 |
| 16 | 14 | SC3 | Serial clock 3 |
| 17 | 15 | $\overline{INT}$ | Active LOW interrupt output |
| 18 | 16 | SCL | Serial clock line |
| 19 | 17 | SDA | Serial data line |
| 20 | 18 | $V_{DD}$ | Supply voltage |

## BLOCK DIAGRAM

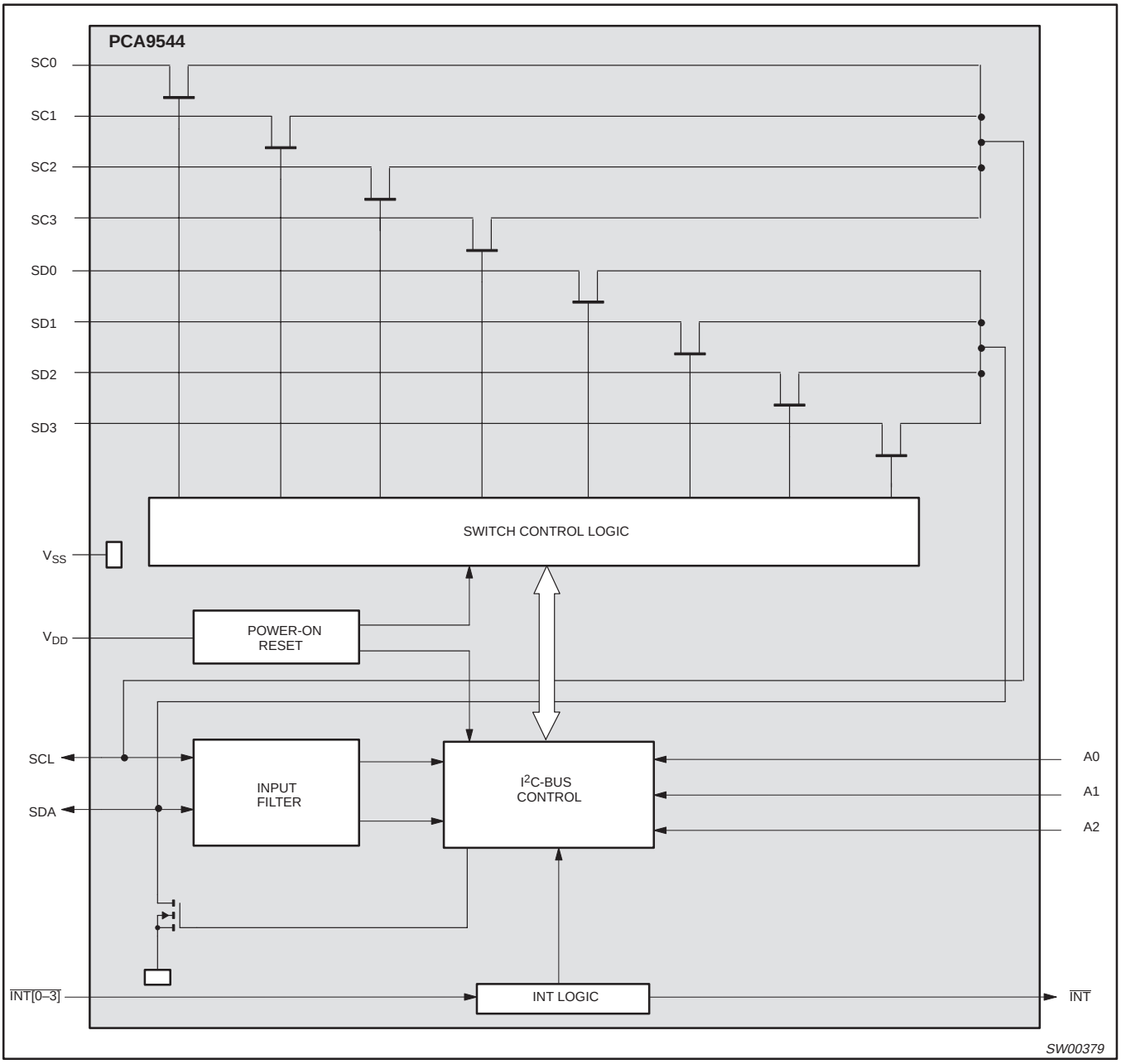



**Figure 3. Block diagram**

## DEVICE ADDRESSING

Following a START condition the bus master must output the address of the slave it is accessing. The address of the PCA9544 is shown in Figure 4. To conserve power, no internal pullup resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

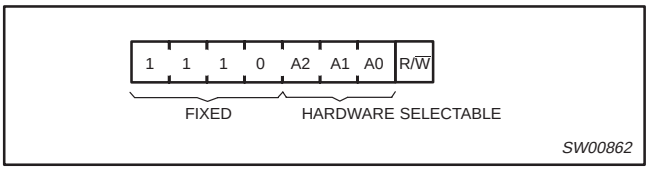



**Figure 4. Slave address**

The last bit of the slave address defines the operation to be performed. When set to logic 1, a read is selected while a logic 0 selects a write operation.

## CONTROL REGISTER

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9544 which will be stored in the Control Register. If multiple bytes are received by the PCA9544, it will save the last byte received. This register can be written and read via the I²C bus.

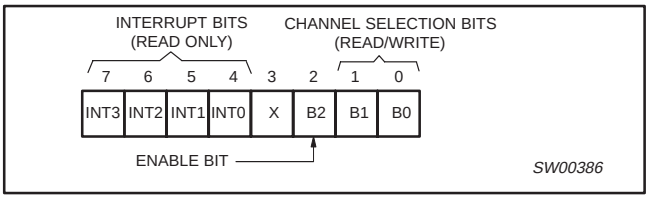



**Figure 5. Control register**

## CONTROL REGISTER DEFINITION

A SCx/SDx downstream pair, or channel, is selected by the contents of the control register. This register is written after the PCA9544 has been addressed. The 3 LSBs of the control byte are used to determine which channel is to be selected. When a channel is selected, it will become active after a stop condition has been placed on the I²C bus. This ensures that all SCx/SDx lines will be in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection.

**Table 1. Control Register; Write — Channel Selection/ Read — Channel Status**

| INT3 | INT2 | INT1 | INT0 | D3 | B2 | B1 | B0 | COMMAND |
|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | 0 | X | X | No channel selected |
| X | X | X | X | X | 1 | 0 | 0 | Channel 0 enabled |
| X | X | X | X | X | 1 | 0 | 1 | Channel 1 enabled |
| X | X | X | X | X | 1 | 1 | 0 | Channel 2 enabled |
| X | X | X | X | X | 1 | 1 | 1 | Channel 3 enabled |

## INTERRUPT HANDLING

The PCA9544 provides 4 interrupt inputs, one for each channel and one open drain interrupt output. When an interrupt is generated by any device, it will be detected by the PCA9544 and the interrupt output will be driven LOW. The channel need not be active for detection of the interrupt. A bit is also set in the control byte. Bits 4 – 7 of the control byte correspond to channels 0 – 3 of the PCA9544, respectively. Therefore, if an interrupt is generated by any device connected to channel 2, the state of the interrupt inputs is loaded into the control register when a read is accomplished. Likewise, an interrupt on any device connected to channel 0 would cause bit 4 of the control register to be set on the read. The master can then address the PCA9544 and read the contents of the control byte to determine which channel contains the device generating the interrupt. The master can then reconfigure the PCA9544 to select this channel, and locate the device generating the interrupt and clear it. The interrupt clears when the device originating the interrupt clears.

It should be noted that more than one device can be providing an interrupt on a channel, so it is up to the master to ensure that all devices on a channel are interrogated for an interrupt.

The interrupt inputs may be used as general purpose inputs if the interrupt function is not required.

If unused, interrupt input(s) must be connected to $V_{DD}$ through a pull-up resistor.

**Table 2. Control Register Read — Interrupt**

| INT3 | INT2 | INT1 | INT0 | D3 | B2 | B1 | B0 | COMMAND |
|---|---|---|---|---|---|---|---|---|
| X | X | X | 0 | X | X | X | X | No interrupt on channel 0 |
| | | | 1 | | | | | Interrupt on channel 0 |
| X | X | 0 | X | X | X | X | X | No interrupt on channel 1 |
| | | 1 | | | | | | Interrupt on channel 1 |
| X | 0 | X | X | X | X | X | X | No interrupt on channel 2 |
| | 1 | | | | | | | Interrupt on channel 2 |
| 0 | X | X | X | X | X | X | X | No interrupt on channel 3 |
| 1 | | | | | | | | Interrupt on channel 3 |

**NOTE:** Several interrupts can be active at the same time.
Ex: INT3 = 0, INT2 = 1, INT1 = 1, INT0 = 0, means that there is no interrupt on channels 0 and 3, and there is interrupt on channels 1 and 2.

## POWER-ON RESET

When power is applied to $V_{DD}$, an internal Power On Reset holds the PCA9544 in a reset state until $V_{DD}$ has reached $V_{POR}$. At this point, the reset condition is released and the PCA9544 registers and I²C state machine are initialized to their default states, all zeroes causing all the channels to be deselected.

## VOLTAGE TRANSLATION

The pass gate transistors of the PCA9544 are constructed such that the $V_{DD}$ voltage can be used to limit the maximum voltage that will be passed from one I²C bus to another.

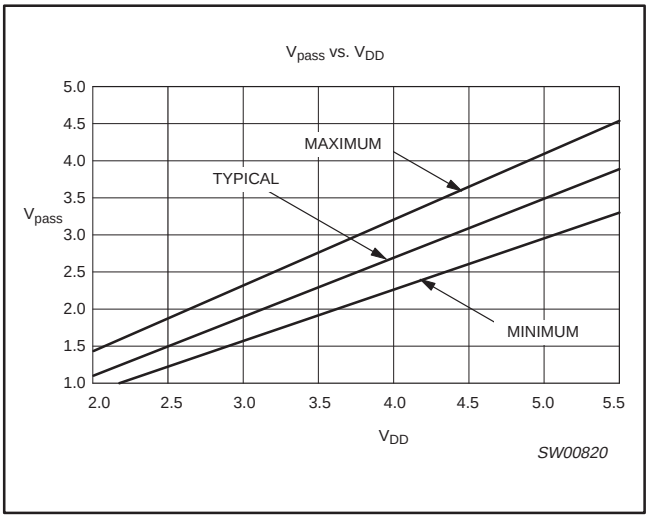



**Figure 6. $V_{pass}$ voltage**

Figure 6 shows the voltage characteristics of the pass gate transistors (note that the graph was generated using the data specified in the DC Characteristics section of this datasheet). In order for the PCA9544 to act as a voltage translator, the $V_{pass}$ voltage should be equal to, or lower than the lowest bus voltage. For example, if the main bus was running at 5 V, and the downstream buses were 3.3 V and 2.7 V, then $V_{pass}$ should be equal to or below 2.7 V to effectively clamp the downstream bus voltages. Looking at Figure 6, we see that $V_{pass}$ (max.) will be at 2.7 V when the PCA9544 supply voltage is 3.5 V or lower so the PCA9544 supply voltage could be set to 3.3 V. Pull-up resistors can then be used to bring the bus voltages to their appropriate levels (see Figure 13).

More Information can be found in Application Note AN262 *PCA954X family of I²C/SMBus multiplexers and switches.*

## CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

### Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 7).

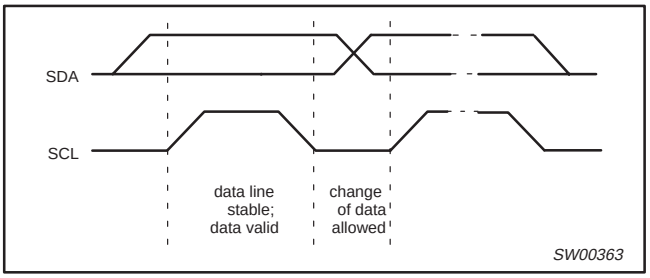



**Figure 7. Bit transfer**

### Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P) (see Figure 8).

### System configuration

A device generating a message is a ‘transmitter’, a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 9).

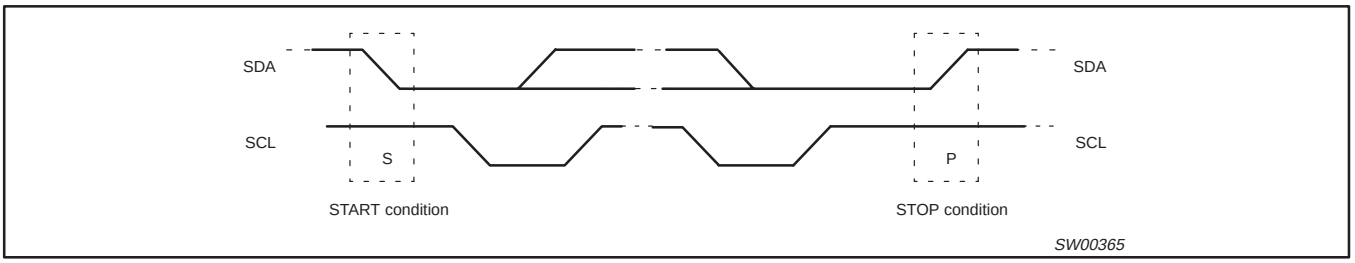



**Figure 8. Definition of start and stop conditions**

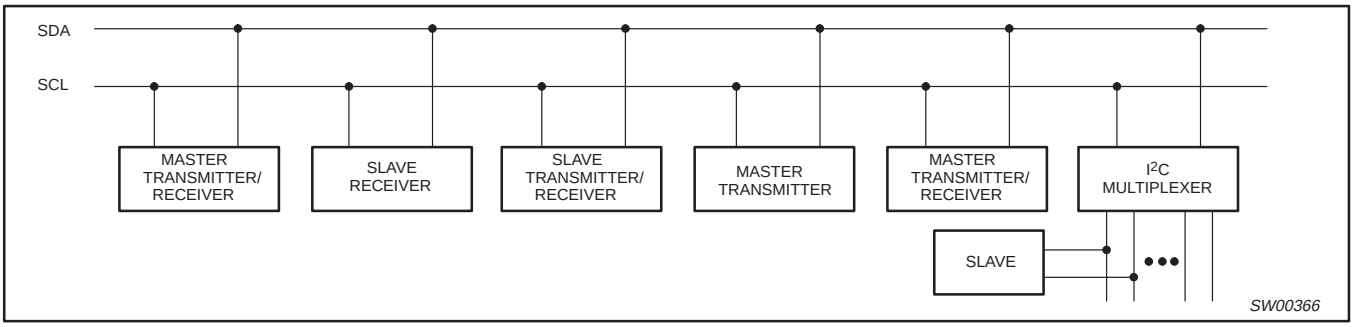



**Figure 9. System configuration**

## Acknowledge

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

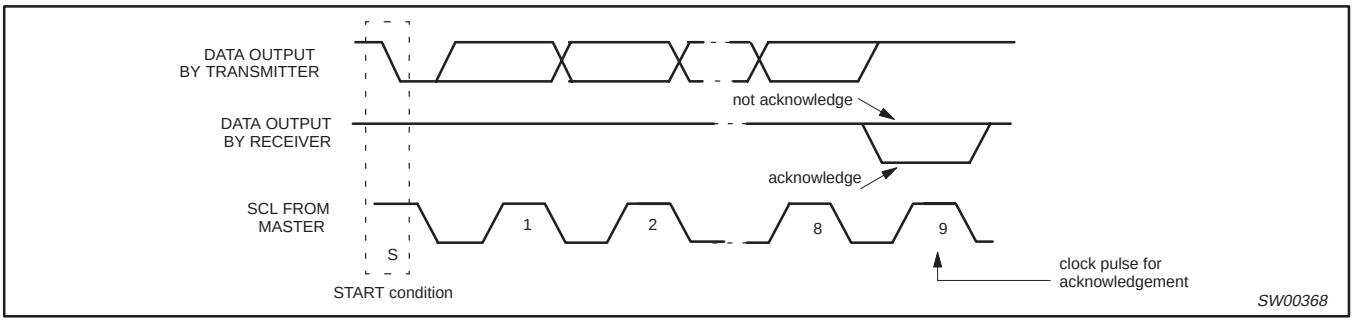



**Figure 10. Acknowledgement on the I²C-bus**

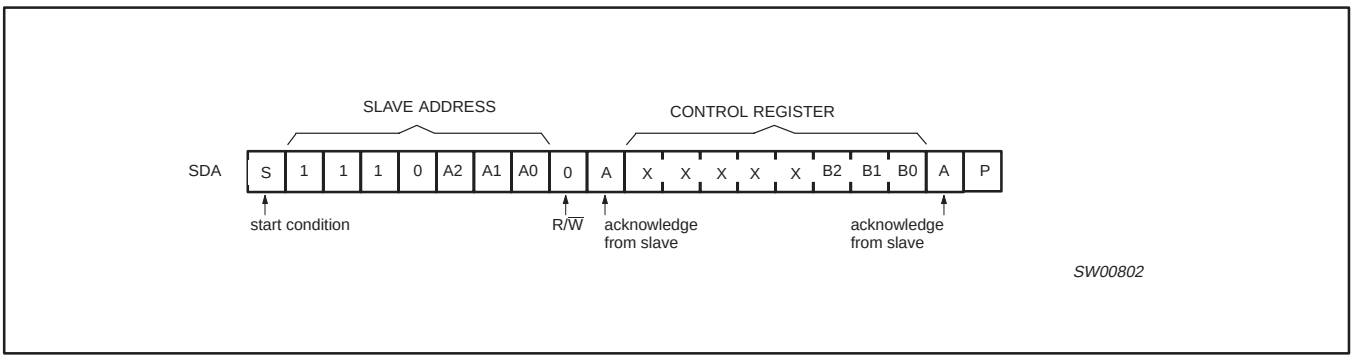



**Figure 11. WRITE control register**

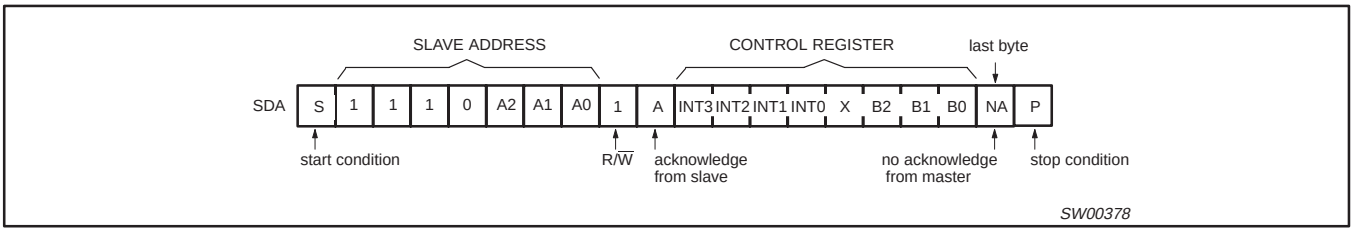
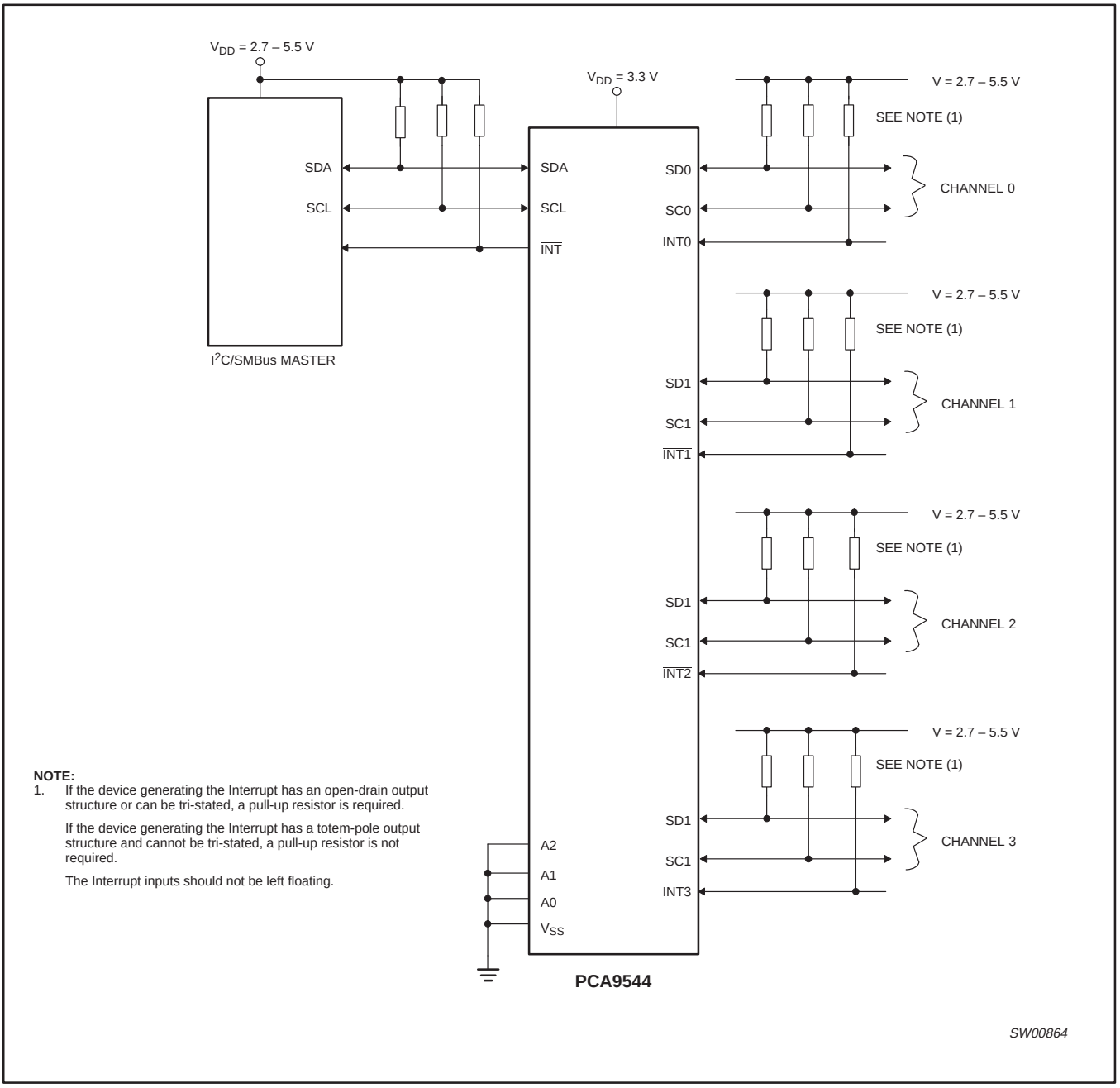



**Figure 12. READ control register**

## TYPICAL APPLICATION




**NOTE:**
1. If the device generating the Interrupt has an open-drain output structure or can be tri-stated, a pull-up resistor is required.

   If the device generating the Interrupt has a totem-pole output structure and cannot be tri-stated, a pull-up resistor is not required.

   The Interrupt inputs should not be left floating.

**Figure 13. Typical application**

## ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).Voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | DC supply voltage | | –0.5 to +7.0 | V |
| $V_I$ | DC input voltage | | –0.5 to +7.0 | V |
| $I_I$ | DC input current | | ±20 | mA |
| $I_O$ | DC output current | | ±25 | mA |
| $I_{DD}$ | Supply current | | ±100 | mA |
| $I_{SS}$ | Supply current | | ±100 | mA |
| $P_{tot}$ | total power dissipation | | 400 | mW |
| $T_{stg}$ | Storage temperature range | | –60 to +150 | °C |
| $T_{amb}$ | Operating ambient temperature | | –40 to +85 | °C |

**NOTES:**

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.

## DC CHARACTERISTICS

$V_{DD}$ = 2.3 to 3.6 V; $V_{SS}$ = 0 V; $T_{amb}$ = –40 °C to +85 °C; unless otherwise specified. (See page 10 for $V_{DD}$ = 3.6 to 5.5 V)

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **Supply** | | | | | | |
| $V_{DD}$ | Supply voltage | | 2.3 | — | 3.6 | V |
| $I_{DD}$ | Supply current | Operating mode; $V_{DD}$ = 3.6 V; no load; $V_I$ = $V_{DD}$ or $V_{SS}$; $f_{SCL}$ = 100 kHz | — | 40 | 100 | µA |
| $I_{stb}$ | Standby current | Standby mode; $V_{DD}$ = 3.6 V; no load; $V_I$ = $V_{DD}$ or $V_{SS}$; $f_{SCL}$ = 0 kHz | — | 25 | 100 | µA |
| $V_{POR}$ | Power-on reset voltage | no load; $V_I$ = $V_{DD}$ or $V_{SS}$ | — | 1.6 | 2.1 | V |
| **Input SCL; input/output SDA** | | | | | | |
| $V_{IL}$ | LOW level input voltage | | –0.5 | — | 0.3 $V_{DD}$ | V |
| $V_{IH}$ | HIGH level input voltage | | 0.7 $V_{DD}$ | — | 6 | V |
| $I_{OL}$ | LOW level output current | $V_{OL}$ = 0.4 V | 3 | — | — | mA |
| | | $V_{OL}$ = 0.6 V | 6 | — | — | |
| $I_L$ | Leakage current | $V_I$ = $V_{DD}$ or $V_{SS}$ | –1 | — | +1 | µA |
| $C_i$ | Input capacitance | $V_I$ = $V_{SS}$ | — | 12 | 13 | pF |
| **Select inputs A0 to A2 / $\overline{INT0}$ to $\overline{INT3}$** | | | | | | |
| $V_{IL}$ | LOW level input voltage | | –0.5 | — | +0.3 $V_{DD}$ | V |
| $V_{IH}$ | HIGH level input voltage | | 0.7 $V_{DD}$ | — | $V_{DD}$ + 0.5 | V |
| $I_{LI}$ | Input leakage current | pin at $V_{DD}$ or $V_{SS}$ | –1 | — | +1 | µA |
| $C_i$ | Input capacitance | $V_I$ = $V_{SS}$ | — | 1.6 | 3 | pF |
| **Pass Gate** | | | | | | |
| $R_{ON}$ | Switch resistance | $V_{CC}$ = 3.0 to 3.6 V, $V_O$ = 0.4 V, $I_O$ = 15 mA | 5 | 20 | 30 | Ω |
| | | $V_{CC}$ = 2.3 to 2.7 V, $V_O$ = 0.4V, $I_O$ = 10 mA | 7 | 26 | 55 | |
| $V_{Pass}$ | Switch output voltage | $V_{swin}$ = $V_{DD}$ = 3.3 V; $I_{swout}$ = –100 µA | — | 2.2 | — | V |
| | | $V_{swin}$ = $V_{DD}$ = 3.0 to 3.6 V; $I_{swout}$ = –100 µA | 1.6 | — | 2.8 | |
| | | $V_{swin}$ = $V_{DD}$ = 2.5 V; $I_{swout}$ = –100 µA | — | 1.5 | — | |
| | | $V_{swin}$ = $V_{DD}$ = 2.3 to 2.7 V; $I_{swout}$ = –100 µA | 1.1 | — | 2.0 | |
| $I_L$ | Leakage current | $V_I$ = $V_{DD}$ or $V_{SS}$ | –1 | — | +1 | µA |
| $C_{io}$ | Input/output capacitance | $V_I$ = $V_{SS}$ | — | 3 | 5 | pF |
| **$\overline{INT}$ Output** | | | | | | |
| $I_{OL}$ | LOW level output current | $V_{OL}$ = 0.4 V | 3 | — | — | mA |
| $I_{OH}$ | HIGH level output current | | — | — | +100 | µA |

## DC CHARACTERISTICS

$V_{DD}$ = 3.6 to 5.5 V; $V_{SS}$ = 0 V; $T_{amb}$ = –40 °C to +85 °C; unless otherwise specified. (See page 9 for $V_{DD}$ = 2.3 to 3.6 V)

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **Supply** | | | | | | |
| $V_{DD}$ | Supply voltage | | 3.6 | — | 5.5 | V |
| $I_{DD}$ | Supply current | Operating mode; $V_{DD}$ = 5.5 V; no load; $V_I$ = $V_{DD}$ or $V_{SS}$; $f_{SCL}$ = 100 kHz | — | 575 | 600 | µA |
| $I_{stb}$ | Standby current | Standby mode; $V_{DD}$ = 5.5 V; no load; $V_I$ = $V_{DD}$ or $V_{SS}$; $f_{SCL}$ = 0 kHz | — | 130 | 300 | µA |
| $V_{POR}$ | Power-on reset voltage | no load; $V_I$ = $V_{DD}$ or $V_{SS}$ | — | 1.7 | 2.1 | V |
| **Input SCL; input/output SDA** | | | | | | |
| $V_{IL}$ | LOW level input voltage | | –0.5 | — | 0.3 $V_{DD}$ | V |
| $V_{IH}$ | HIGH level input voltage | | 0.7 $V_{DD}$ | — | 6 | V |
| $I_{OL}$ | LOW level output current | $V_{OL}$ = 0.4 V | 3 | — | — | mA |
| | | $V_{OL}$ = 0.6 V | 6 | — | — | mA |
| $I_{IL}$ | Low level input current | $V_I$ = $V_{SS}$ | –10 | — | +10 | µA |
| $I_{IH}$ | HIGH level input current | $V_I$ = $V_{DD}$ | — | — | 100 | µA |
| $C_i$ | Input capacitance | $V_I$ = $V_{SS}$ | — | 12 | 13 | pF |
| **Select inputs A0 to A2 / $\overline{INT0}$ to $\overline{INT3}$** | | | | | | |
| $V_{IL}$ | LOW level input voltage | | –0.5 | — | +0.3 $V_{DD}$ | V |
| $V_{IH}$ | HIGH level input voltage | | 0.7 $V_{DD}$ | — | $V_{DD}$ + 0.5 | V |
| $I_{LI}$ | Input leakage current | pin at $V_{DD}$ or $V_{SS}$ | –1 | — | +50 | µA |
| $C_i$ | Input capacitance | $V_I$ = $V_{SS}$ | — | 2 | 5 | pF |
| **Pass Gate** | | | | | | |
| $R_{ON}$ | Switch resistance | $V_{CC}$ = 4.5 to 5.5 V, $V_O$ = 0.4 V, $I_O$ = 15 mA | 4 | 11 | 24 | Ω |
| $V_{Pass}$ | Switch output voltage | $V_{swin}$ = $V_{DD}$ = 5.0 V; $I_{swout}$ = –100 µA | — | 3.5 | — | V |
| | | $V_{swin}$ = $V_{DD}$ = 4.5 to 5.5 V; $I_{swout}$ = –100 µA | 2.6 | – | 4.5 | V |
| $I_L$ | Leakage current | $V_I$ = $V_{DD}$ or $V_{SS}$ | –10 | — | +100 | µA |
| $C_{io}$ | Input/output capacitance | $V_I$ = $V_{SS}$ | — | 3 | 5 | pF |
| **$\overline{INT}$ Output** | | | | | | |
| $I_{OL}$ | LOW level output current | $V_{OL}$ = 0.4 V | 3 | — | — | mA |
| $I_{OH}$ | HIGH level output current | | — | — | +100 | µA |

## AC CHARACTERISTICS

| SYMBOL | PARAMETER | STANDARD-MODE I²C-BUS | | FAST-MODE I²C-BUS | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | Propagation delay from SDA to $SD_n$ or SCL to $SC_n$ | — | 0.3[1] | — | 0.3[1] | ns |
| $f_{SCL}$ | SCL clock frequency | 0 | 100 | 0 | 400 | kHz |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 4.7 | — | 1.3 | — | µs |
| $t_{HD;STA}$ | Hold time (repeated) START condition<br>After this period, the first clock pulse is generated | 4.0 | — | 0.6 | — | µs |
| $t_{LOW}$ | LOW period of the SCL clock | 4.7 | — | 1.3 | — | µs |
| $t_{HIGH}$ | HIGH period of the SCL clock | 4.0 | — | 0.6 | — | µs |
| $t_{SU;STA}$ | Set-up time for a repeated START condition | 4.7 | — | 0.6 | — | µs |
| $t_{SU;STO}$ | Set-up time for STOP condition | 4.0 | — | 0.6 | — | µs |
| $t_{HD;DAT}$ | Data hold time | 0[2] | 3.45 | 0[2] | 0.9 | µs |
| $t_{SU;DAT}$ | Data set-up time | 250 | — | 100 | — | ns |
| $t_R$ | Rise time of both SDA and SCL signals | — | 1000 | $20 + 0.1C_b$[3] | 300 | ns |
| $t_F$ | Fall time of both SDA and SCL signals | — | 300 | $20 + 0.1C_b$[3] | 300 | µs |
| $C_b$ | Capacitive load for each bus line | — | 400 | — | 400 | µs |
| $t_{SP}$ | Pulse width of spikes which must be suppressed by the input filter | — | 50 | — | 50 | ns |
| $t_{VD:DATL}$ | Data valid (HL) | — | 1 | — | 1 | µs |
| $t_{VD:DATH}$ | Data valid (LH) | — | 0.6 | — | 0.6 | µs |
| $t_{VD:ACK}$ | Data valid Acknowledge | — | 1 | — | 1 | µs |
| $\overline{INT}$ | | | | | | |
| $t_{iv}$ | $\overline{INTn}$ to $\overline{INT}$ active valid time | — | 4 | — | 4 | µs |
| $t_{ir}$ | $\overline{INTn}$ to $\overline{INT}$ inactive delay time | — | 2 | — | 2 | µs |
| $L_{pwr}$ | LOW level pulse width rejection or $\overline{INTn}$ inputs | 10 | — | 1 | — | ns |
| $H_{pwr}$ | HIGH level pulse width rejection or $\overline{INTn}$ inputs | 500 | — | 500 | — | ns |

**NOTES:**
1. Pass gate propagation delay is calculated from the 20 Ω typical $R_{ON}$ and and the 15 pF load capacitance.
2. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $VIH_{min}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
3. $C_b$ = total capacitance of one bus line in pF.

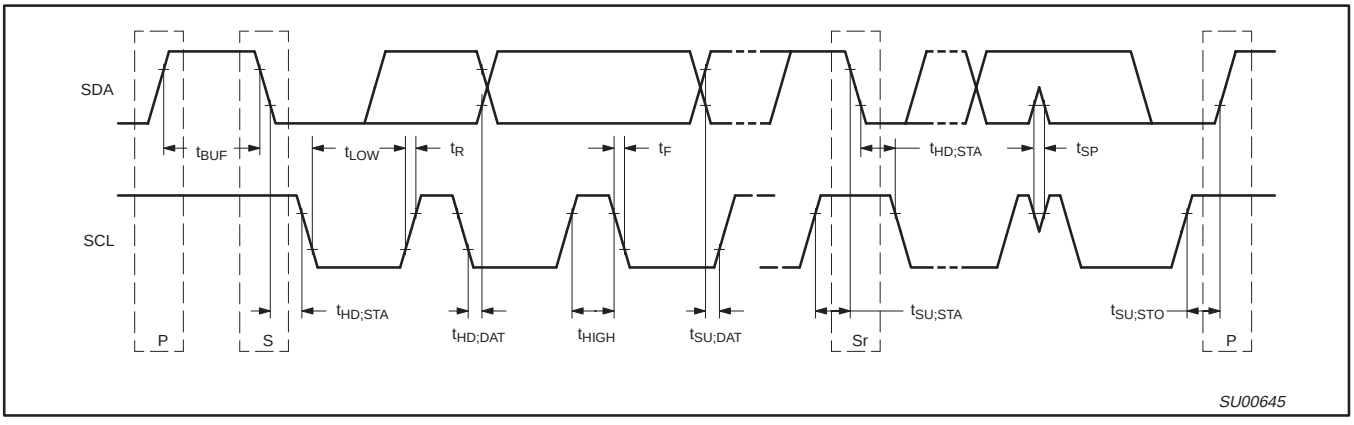
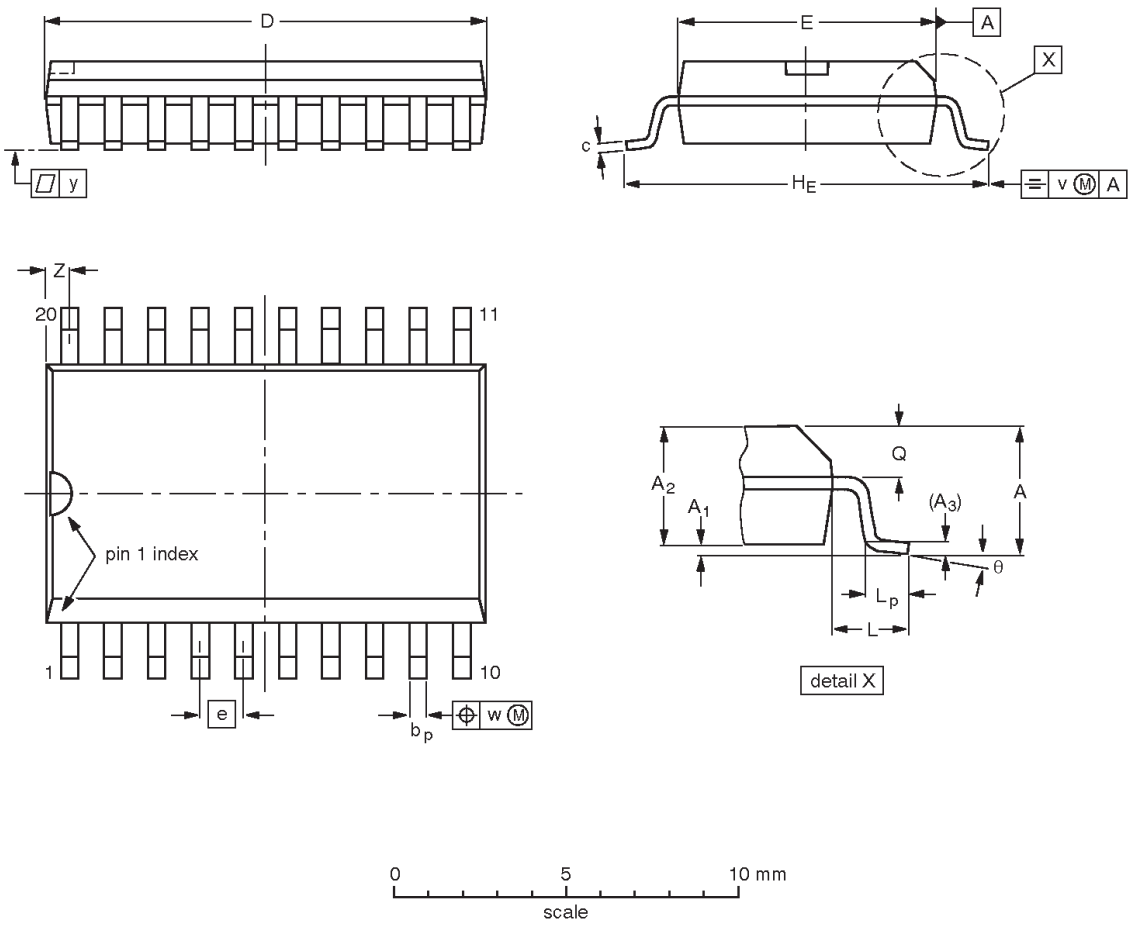



**Figure 14. Definition of timing on the I²C-bus**

**SO20: plastic small outline package; 20 leads; body width 7.5 mm** **SOT163-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

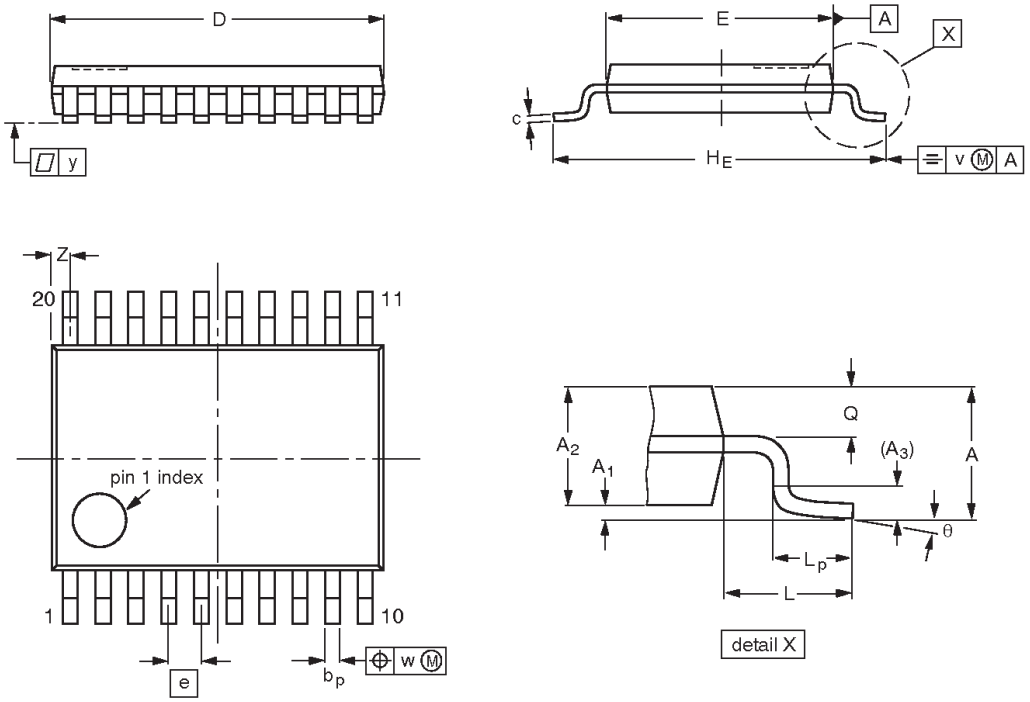
| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.65 | 0.30<br>0.10 | 2.45<br>2.25 | 0.25 | 0.49<br>0.36 | 0.32<br>0.23 | 13.0<br>12.6 | 7.6<br>7.4 | 1.27 | 10.65<br>10.00 | 1.4 | 1.1<br>0.4 | 1.1<br>1.0 | 0.25 | 0.25 | 0.1 | 0.9<br>0.4 | $8^o$<br>$0^o$ |
| inches | 0.10 | 0.012<br>0.004 | 0.096<br>0.089 | 0.01 | 0.019<br>0.014 | 0.013<br>0.009 | 0.51<br>0.49 | 0.30<br>0.29 | 0.050 | 0.419<br>0.394 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016 | |

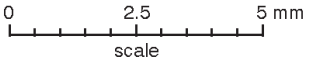
**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT163-1 | 075E04 | MS-013 | | | | ~~97-05-22~~<br>99-12-27 |

**TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm** **SOT360-1**




**DIMENSIONS (mm are the original dimensions)**

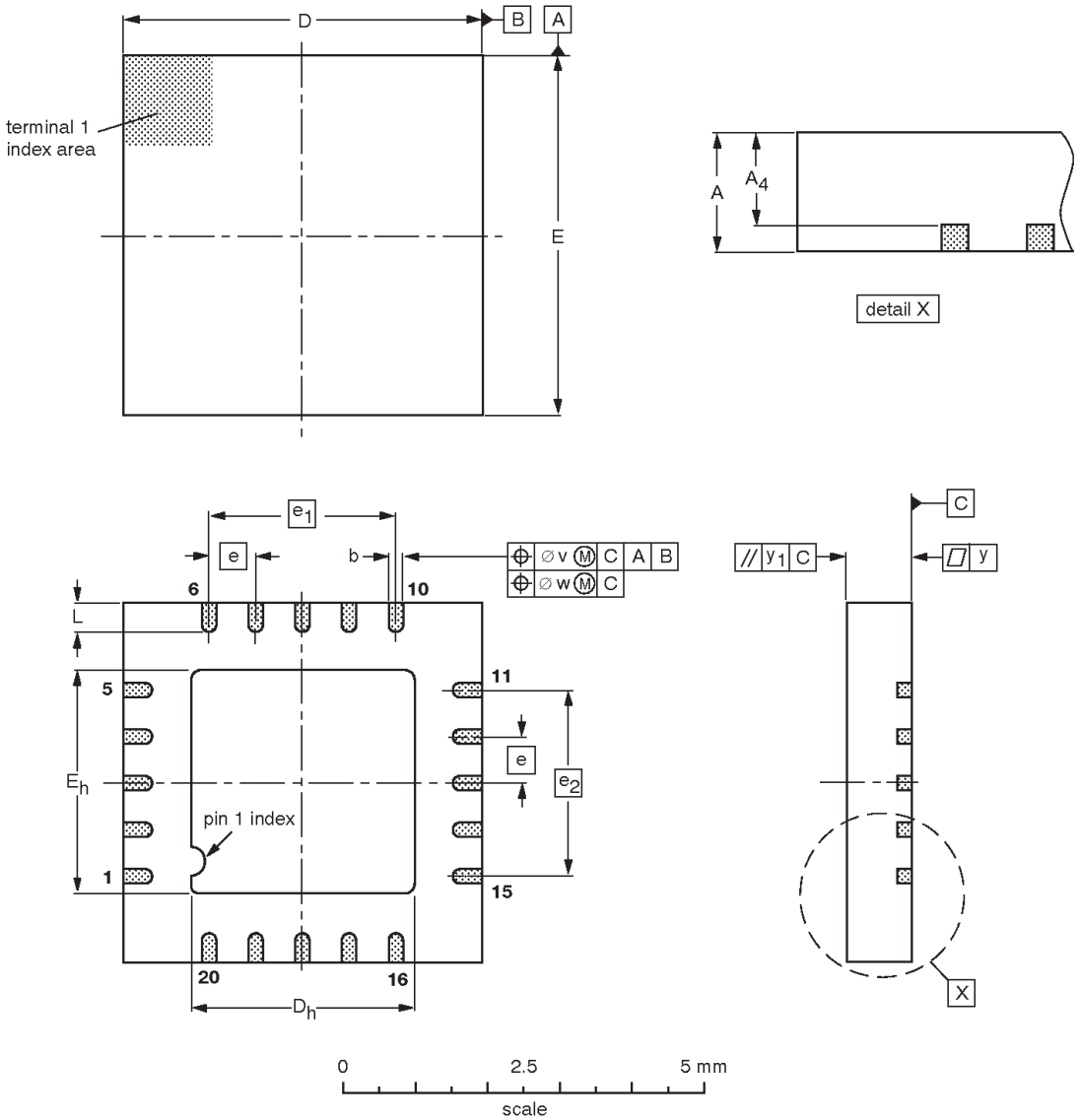
| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.10 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 6.6<br>6.4 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1.0 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.5<br>0.2 | 8°<br>0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT360-1 | | MO-153 | | | | ~~95-02-04~~<br>99-12-27 |

**HVQFN20: plastic, heatsink very thin quad flat package; no leads; 20 terminals; body 5 x 5 x 0.85 mm** **SOT662-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_4$ max. | b | D(1) | $D_h$ | E(1) | $E_h$ | e | $e_1$ | $e_2$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.00 | 0.80 | 0.40<br>0.23 | 5.05<br>4.95 | 3.25<br>2.95 | 5.05<br>4.95 | 3.25<br>2.95 | 0.65 | 2.6 | 2.6 | 0.75<br>0.50 | 0.2 | 0.1 | 0.05 | 0.1 |

**Note**

1. Plastic or metal protrusions of 0.076 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT662-1 | | MO-220 | | | | ~~01-06-28~~<br>01-08-08 |

# 4-channel I²C multiplexer with interrupt logic PCA9544

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

## Data sheet status

| Data sheet status[1] | Product status[2] | Definitions |
|---|---|---|
| Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
| Product data | Production | This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A. |

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

## Definitions

**Short-form specification —** The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition —** Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information —** Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

## Disclaimers

**Life support —** These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

**Right to make changes —** Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

## Contact information

For additional information please visit
**http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to:
**sales.addresses@www.semiconductors.philips.com**.



Date of release: 07-02

Document order number: 9397 750 10162

Let's make things better.

**Philips Semiconductors**

PHILIPS