

PHP/PHB/PHD14NQ20T

TrenchMOS™ standard level FET

Rev. 03 — 11 March 2002

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PHP14NQ20T in SOT78 (TO-220AB)

PHB14NQ20T in SOT404 (D²-PAK)

PHD14NQ20T in SOT428 (D-PAK).

1.2 Features

- Low on-state resistance
- Fast switching

1.3 Applications

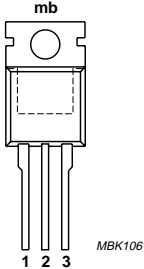
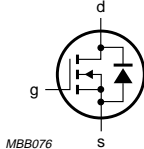
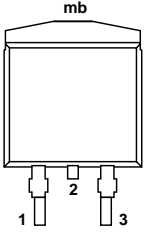
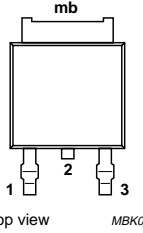
- DC to DC converters
- General purpose switching

1.4 Quick reference data

- $V_{DS} = 200\text{ V}$
- $I_D = 14\text{ A}$
- $R_{DS(on)} \leq 230\text{ m}\Omega$
- $P_D = 125\text{ W}$

2. Pinning information

Table 1: Pinning - SOT78, SOT404, SOT428, simplified outline and symbol

| Pin | Description | Simplified outline | Symbol | |
|-----|--|--|---|-----------------------|
| 1 | gate (g) |  |  | |
| 2 | drain (d) [1] | | | |
| 3 | source (s) | | | |
| mb | mounting base, connected to drain (d) |  MBK116 | MBB076 | |
| | |  Top view MBK091 | | |
| | | | | |
| | | SOT78 (TO-220AB) | SOT404 (D²-PAK) | SOT428 (D-PAK) |

[1] It is not possible to make connection to pin 2 of the SOT404 or SOT428 packages.



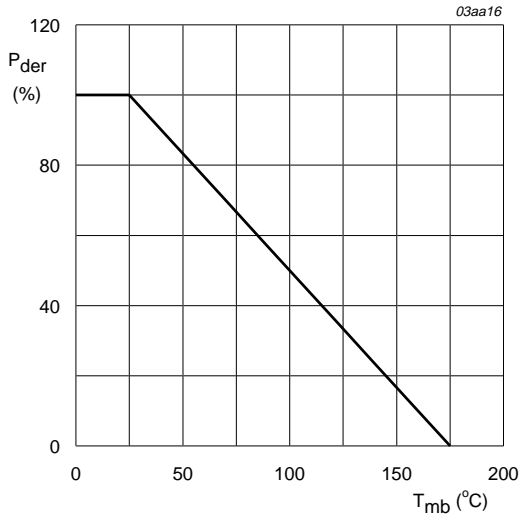
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3. Limiting values

Table 2: Limiting values

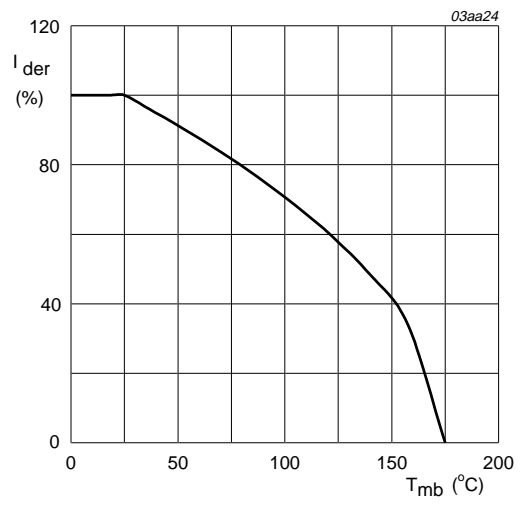
In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------------------|---------------------------------------|--|-----|----------|--------|
| V_{DS} | drain-source voltage (DC) | $T_j = 25$ to 175 °C | - | 200 | V |
| V_{DGR} | drain-gate voltage (DC) | $T_j = 25$ to 175 °C; $R_{GS} = 20$ k Ω | - | 200 | V |
| V_{GS} | gate-source voltage | | - | ± 20 | V |
| I_D | drain current (DC) | $V_{GS} = 10$ V; Figure 2 and 3 $T_{mb} = 25$ °C $T_{mb} = 100$ °C | - | 14 10 | A A |
| I_{DM} | peak drain current | $T_{mb} = 25$ °C; pulsed; $t_p \leq 10$ μ s; Figure 3 | - | 56 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25$ °C; Figure 1 | - | 125 | W |
| T_{stg} | storage temperature | | -55 | +175 | °C |
| T_j | operating junction temperature | | -55 | +175 | °C |
| Source-drain diode | | | | | |
| I_S | source (diode forward) current (DC) | $T_{mb} = 25$ °C | - | 14 | A |
| I_{SM} | peak source (diode forward) current | $T_{mb} = 25$ °C; pulsed; $t_p \leq 10$ μ s | - | 56 | A |
| Avalanche ruggedness | | | | | |
| $E_{DS(ALS)}$ | non-repetitive avalanche energy | unclamped inductive load; $I_D = 14$ A; | - | 70 | mJ |
| $I_{DS(ALM)}$ | peak non-repetitive avalanche current | $t_p = 20$ μ s; $V_{DD} \leq 25$ V; $R_{GS} = 50$ Ω ; $V_{GS} = 10$ V; starting $T_j = 25$ °C; Figure 15 | - | 14 | A |



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

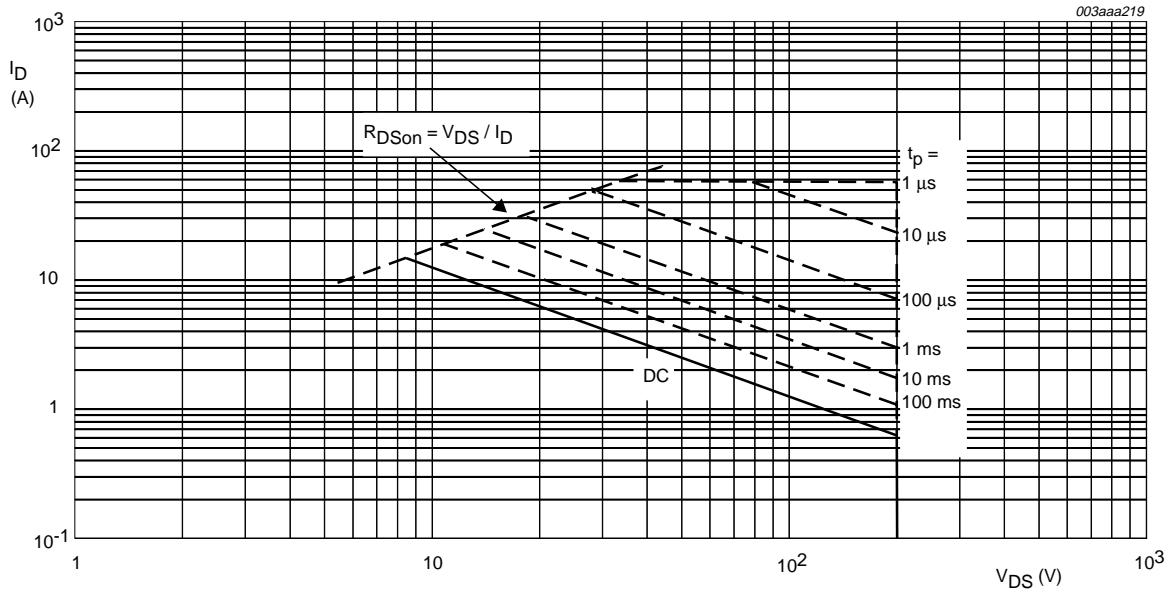
Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$V_{GS} \geq 10 \text{ V}$$

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^{\circ}C$; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

4. Thermal characteristics

Table 3: Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---|---|-----|-----|-----|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Figure 4 | - | - | 1.2 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | vertical in still air; SOT78 package | - | 60 | - | K/W |
| | | SOT404 and SOT428 packages; SOT404 minimum footprint; mounted on a PCB | - | 50 | - | K/W |

4.1 Transient thermal impedance

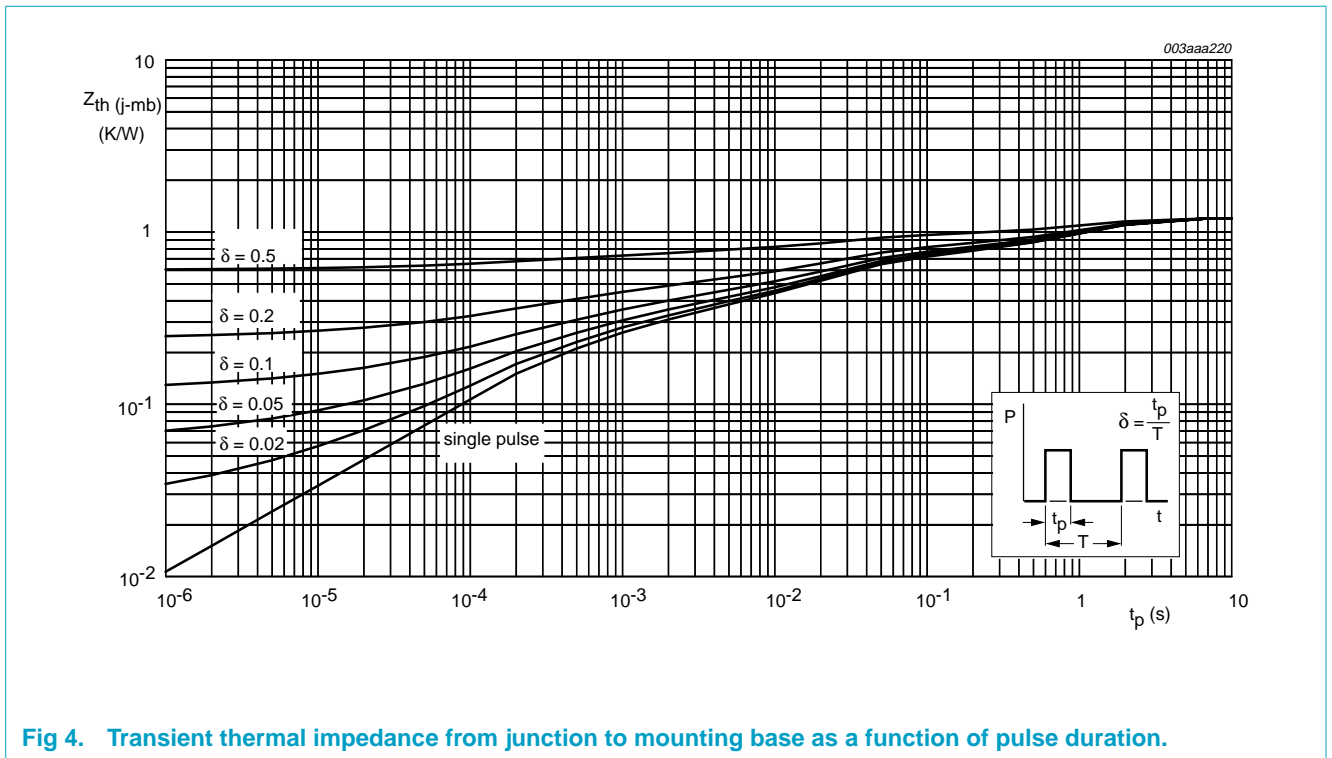
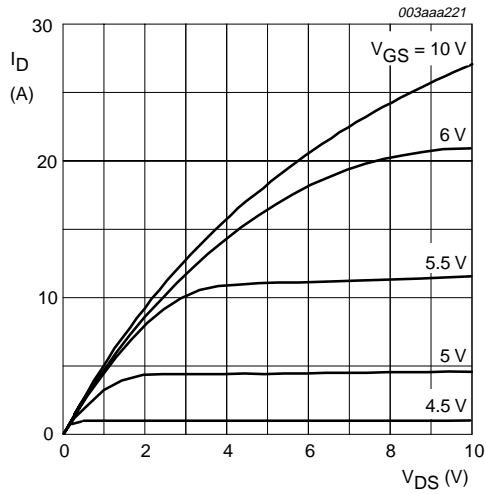


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

5. Characteristics

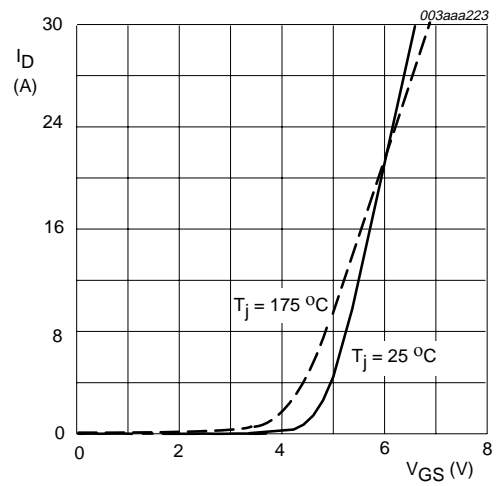
Table 4: Characteristics
 $T_j = 25\text{ °C}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|--------------------------------------|---|-----|------|-----|---------------|
| Static characteristics | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$ | 200 | - | - | V |
| | | $T_j = -55\text{ °C}$ | 178 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; Figure 9 | | | | |
| | | $T_j = 25\text{ °C}$ | 2 | 3 | 4 | V |
| | | $T_j = 175\text{ °C}$ | 1 | - | - | V |
| | | $T_j = -55\text{ °C}$ | - | - | 6 | V |
| I_{DSS} | drain-source leakage current | $V_{DS} = 200\ \text{V}$; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$ | - | 0.05 | 10 | μA |
| | | $T_j = 175\text{ °C}$ | - | - | 500 | μA |
| I_{GSS} | gate-source leakage current | $V_{GS} = \pm 10\ \text{V}$; $V_{DS} = 0\ \text{V}$ | - | 10 | 100 | nA |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 10\ \text{V}$; $I_D = 7\ \text{A}$; Figure 7 and 8 | | | | |
| | | $T_j = 25\text{ °C}$ | - | 150 | 230 | m Ω |
| | | $T_j = 175\text{ °C}$ | - | - | 633 | m Ω |
| Dynamic characteristics | | | | | | |
| g_{fs} | forward transconductance | $V_{DS} = 25\ \text{V}$; $I_D = 7\ \text{A}$; Figure 14 | 6 | 12.1 | - | S |
| $Q_{g(tot)}$ | total gate charge | $I_D = 14\ \text{A}$; $V_{DD} = 160\ \text{V}$; | - | 38 | - | nC |
| Q_{gs} | gate-source charge | $V_{GS} = 10\ \text{V}$; Figure 13 | - | 4 | - | nC |
| Q_{gd} | gate-drain (Miller) charge | | - | 13.3 | - | nC |
| C_{iss} | input capacitance | $V_{GS} = 0\ \text{V}$; $V_{DS} = 25\ \text{V}$; | - | 1500 | - | pF |
| C_{oss} | output capacitance | $f = 1\ \text{MHz}$; Figure 11 | - | 128 | - | pF |
| C_{rss} | reverse transfer capacitance | | - | 60 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DD} = 30\ \text{V}$; $R_D = 10\ \Omega$; | - | 25 | - | ns |
| t_r | rise time | $V_{GS} = 10\ \text{V}$; $R_{GS} = 50\ \Omega$; | - | 40 | - | ns |
| $t_{d(off)}$ | turn-off delay time | $R_{gen} = 50\ \Omega$ | - | 83 | - | ns |
| t_f | fall time | | - | 31 | - | ns |
| Source-drain diode | | | | | | |
| V_{SD} | source-drain (diode forward) voltage | $I_S = 14\ \text{A}$; $V_{GS} = 0\ \text{V}$; Figure 12 | - | 1.0 | 1.5 | V |
| t_{rr} | reverse recovery time | $I_S = 14\ \text{A}$; | - | 135 | - | ns |
| Q_r | recovered charge | $di_S/dt = -100\ \text{A}/\mu\text{s}$; $V_{GS} = 0\ \text{V}$; $V_R = 30\ \text{V}$ | - | 690 | - | nC |



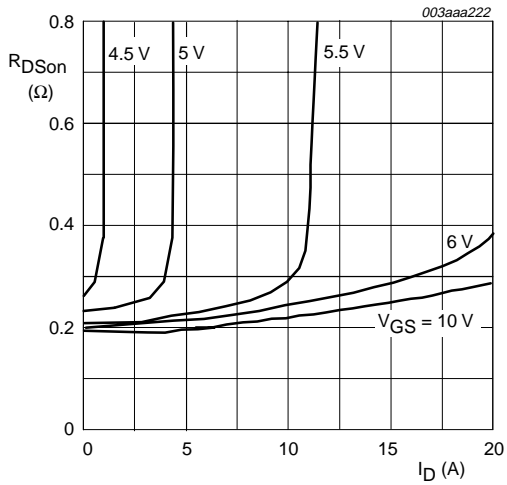
$T_j = 25\text{ °C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



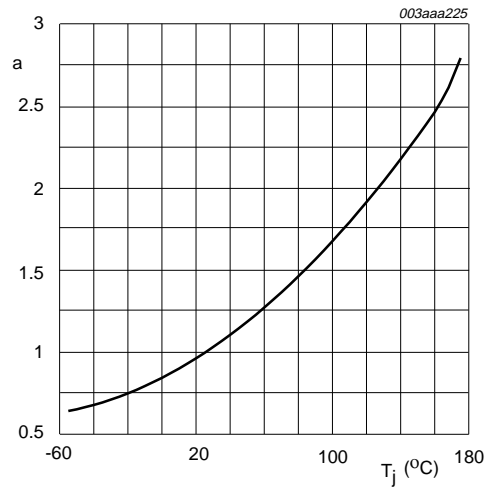
$T_j = 25\text{ °C}$ and 175 °C ; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



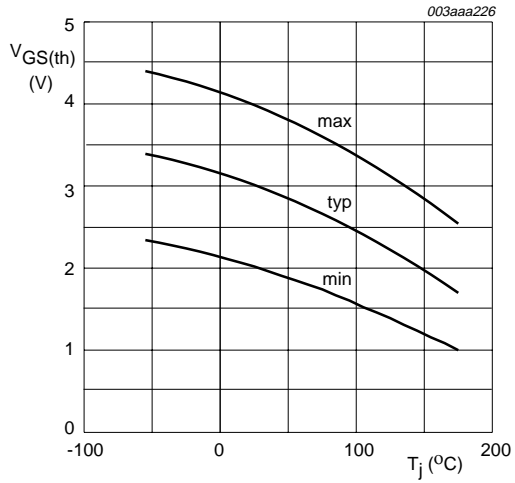
$T_j = 25\text{ °C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



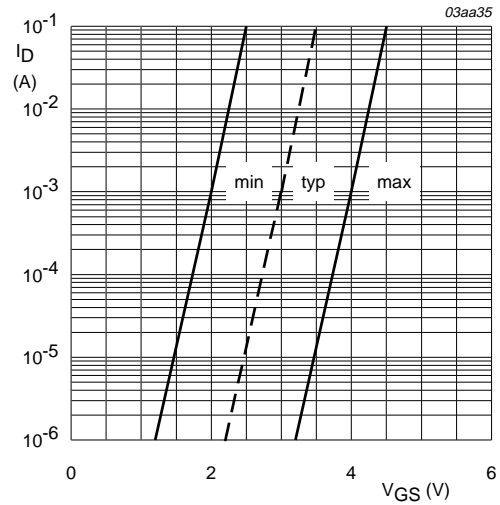
$$a = \frac{R_{DSon}}{R_{DSon(25\text{ °C})}}$$

Fig 8. Normalized drain source on-state resistance factor as a function of junction temperature.



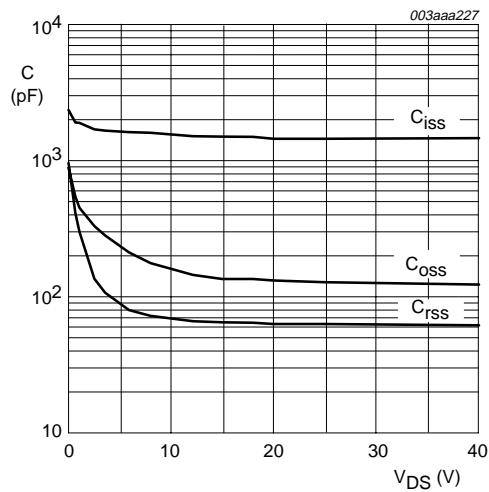
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



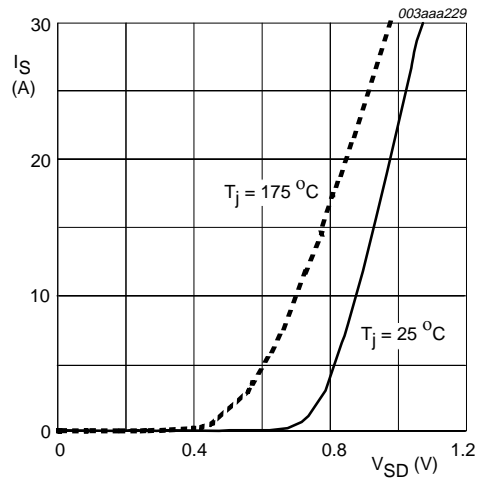
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



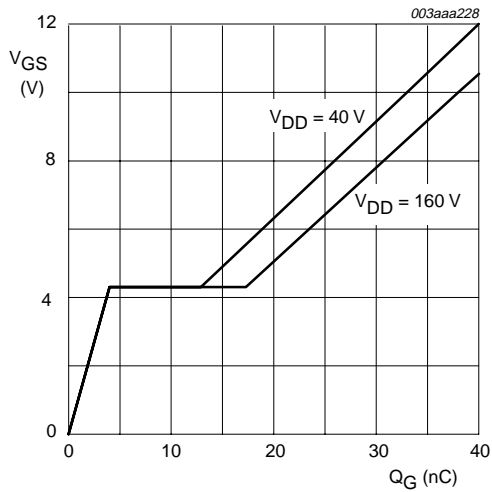
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



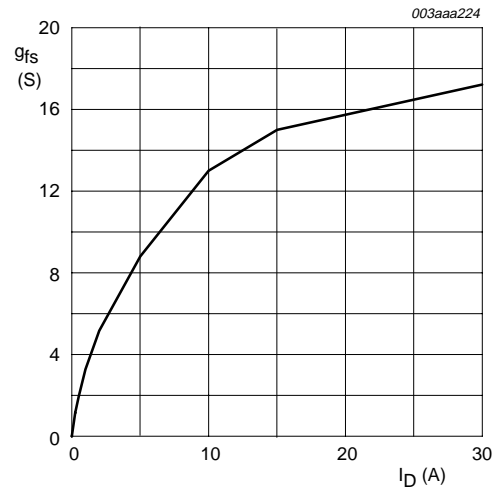
$T_j = 25 \text{ }^{\circ}C \text{ and } 175 \text{ }^{\circ}C; V_{GS} = 0 \text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



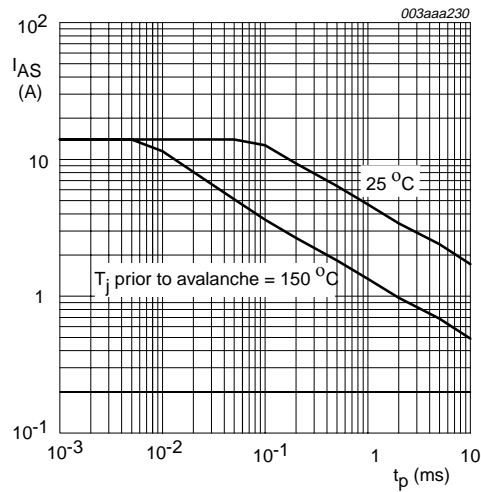
$I_D = 15$ A; $V_{DD} = 40$ V and 160 V

Fig 13. Gate-source voltage as a function of gate charge; typical values.



$V_{DS} = 25$ V

Fig 14. Forward transconductance as a function of drain current; typical values.



Unclamped inductive load; $V_{DD} \leq 25$ V; $R_{GS} = 50$ Ω ; $V_{GS} = 10$ V; starting $T_j = 25$ °C and 150 °C

Fig 15. Non-repetitive avalanche ruggedness current as a function of pulse duration; typical values.

6. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78

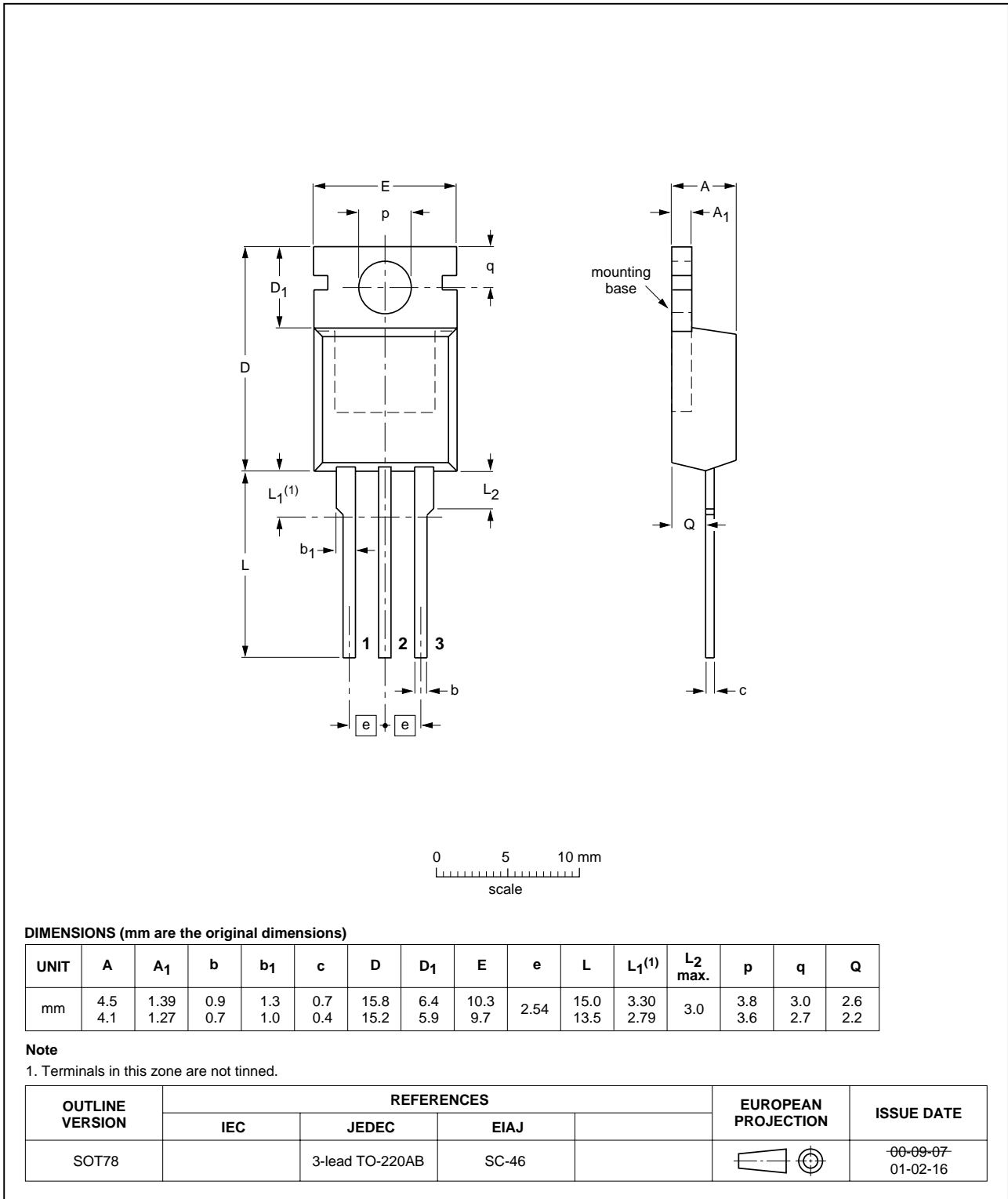


Fig 16. SOT78 (TO-220AB).

Plastic single-ended surface mounted package (Philips version of D²-PAK); 3 leads
(one lead cropped)

SOT404

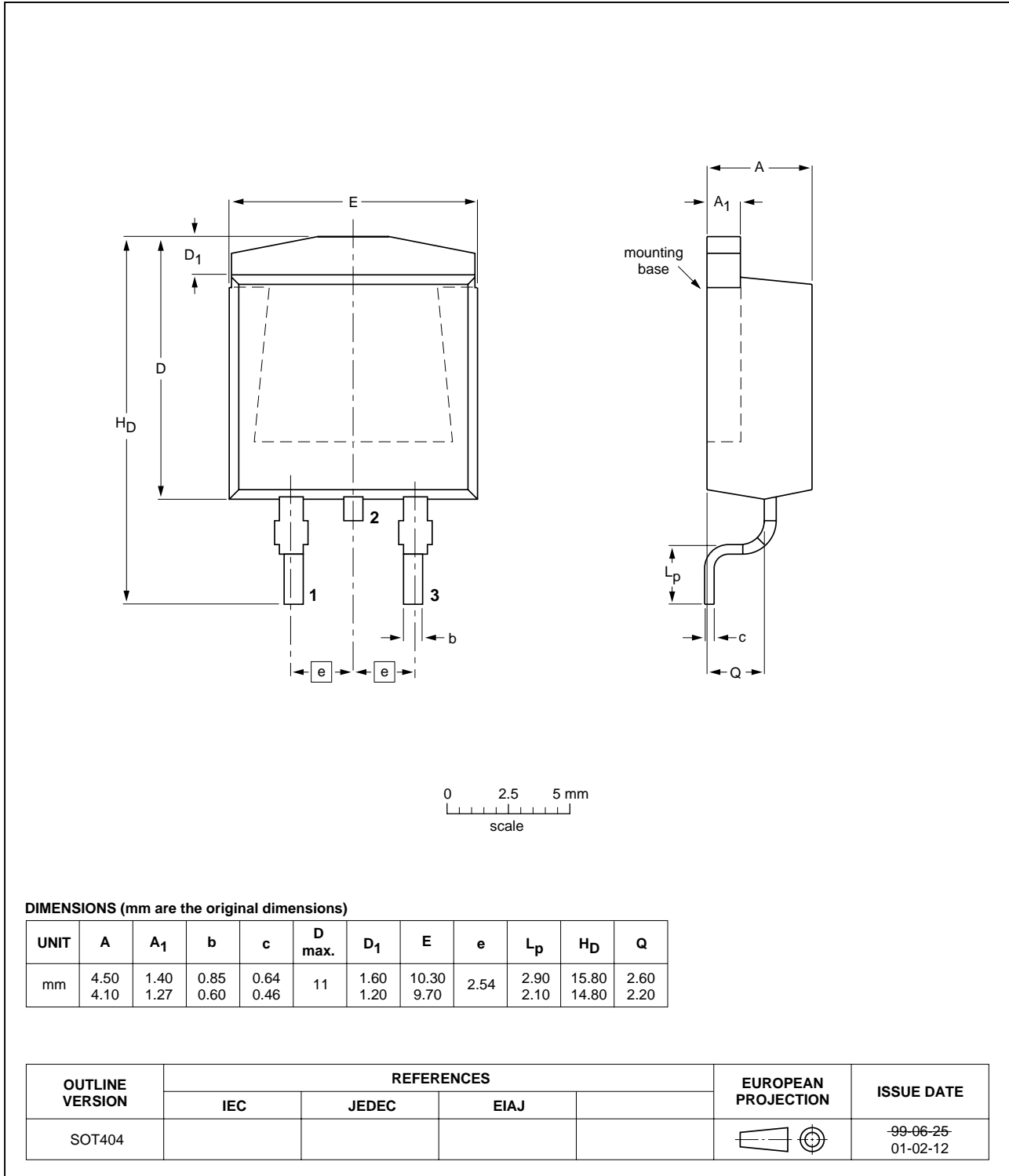


Fig 17. SOT404 (D²-PAK).

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads
(one lead cropped)

SOT428

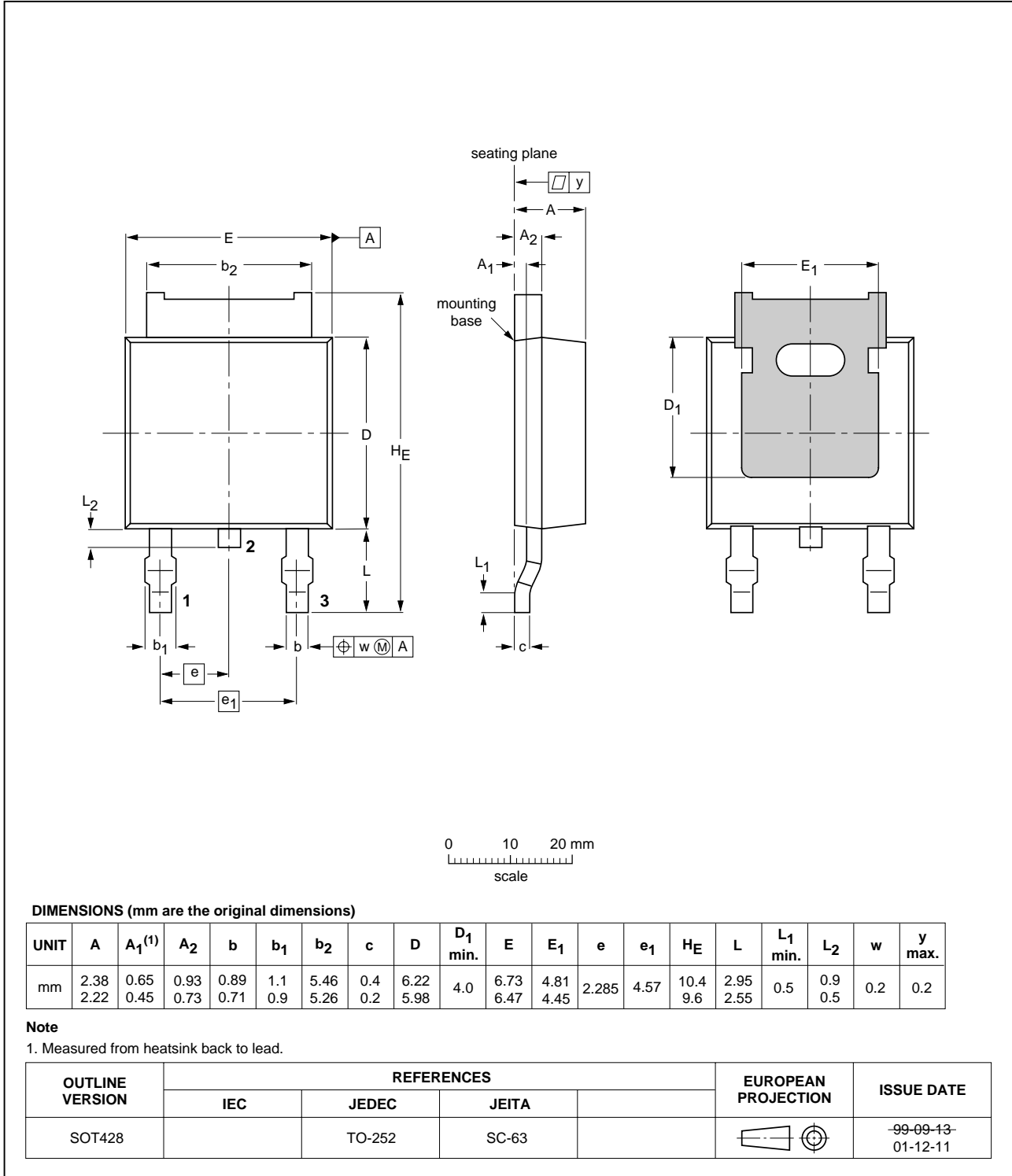


Fig 18. SOT428 (D-PAK).

7. Revision history

Table 5: Revision history

| Rev | Date | CPCN | Description |
|-----|----------|------|--|
| 03 | 20020311 | | Product data; third version. Supersedes data of 6 March 2002. Modifications: <ul style="list-style-type: none">• Correction to product title: PHD14NQ20T. |
| 02 | 20020306 | | Product data; second version. Supersedes initial version of 1 October 1999. Modifications: <ul style="list-style-type: none">• PHD14NQ20T added. |
| 01 | 19991001 | | Product data; initial version |

8. Data sheet status

| Data sheet status ^[1] | Product status ^[2] | Definition |
|----------------------------------|-------------------------------|--|
| Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
| Product data | Production | This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A. |

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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