

PHKD6N02LT

Dual N-channel enhancement mode field effect transistor

Rev. 01 — 07 September 2001

Product data

1. Description

Dual N-channel enhancement mode field-effect transistors within a plastic package using **TrenchMOS™¹** technology.

Product availability:

PHKD6N02LT in SOT96-1 (SO8).

2. Features

- Low on-state resistance
- Surface mount package.

3. Applications

- Notebook computers
- Portable appliances
- Battery chargers.

4. Pinning information

Table 1: Pinning - SOT96-1, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	source1 (s1)	<p>Top view MBK187</p>	<p>MBK725</p>
2	gate1 (g1)		
3	source2 (s2)		
4	gate2 (g2)		
5, 6	drain2 (d2)		
7, 8	drain1 (d1)		

1. TrenchMOS is a trademark of Koninklijke Philips Electronics N.V.



5. Quick reference data

Table 2: Quick reference data

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25$ to 150 °C	–	20	V
I_D	drain current (DC)	$T_{sp} = 25$ °C	–	6	A
P_{tot}	total power dissipation	$T_{sp} = 25$ °C	–	2	W
T_j	junction temperature		–	150	°C
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5$ V; $I_D = 3$ A	16	20	mΩ
		$V_{GS} = 2.5$ V; $I_D = 3$ A	36	45	mΩ

6. Limiting values

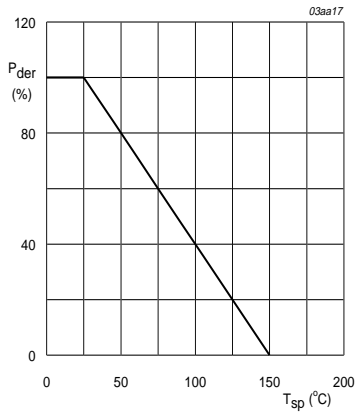
Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25$ to 150 °C	–	20	V
V_{DGR}	drain-gate voltage (DC)	$T_j = 25$ to 150 °C; $R_{GS} = 20$ kΩ	–	20	V
V_{GS}	gate-source voltage (DC)		–	±12	V
I_D	drain current (DC)	$T_{sp} = 25$ °C; Figure 2 and 3	–	6	A
I_{DM}	peak drain current	$T_{sp} = 25$ °C; $t_p \leq 1$ ms; Figure 2 and 3	–	24	A
P_{tot}	total power dissipation	$T_{sp} = 25$ °C; Figure 1	–	2	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C

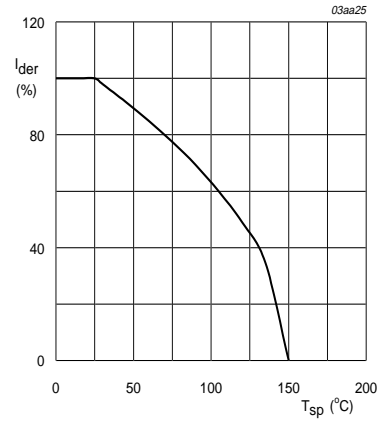
Source-drain (reverse) diode

I_S	source (diode forward) current (DC)	$T_{sp} = 25$ °C	–	6	A
I_{SM}	peak (diode forward) source current	$T_{sp} = 25$ °C; $t_p \leq 10$ μs	–	24	A



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

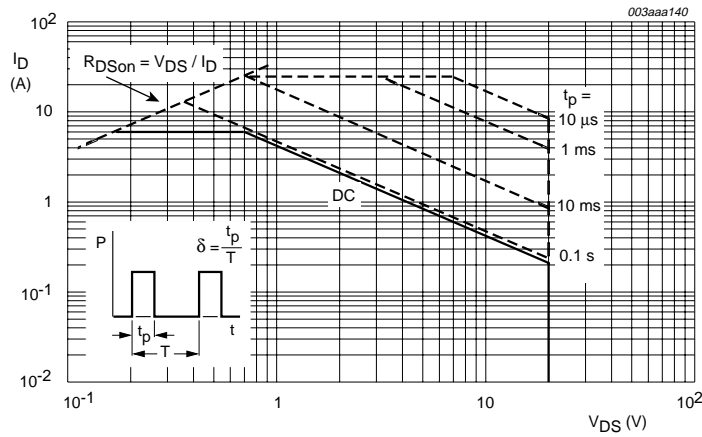
Fig 1. Normalized total power dissipation as a function of solder point temperature.



$V_{GS} \geq 4.5\text{ V}$

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



$T_{sp} = 25^{\circ}C$; I_{DM} is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	mounted on a printed circuit board; minimum footprint; Figure 4	30	K/W

7.1 Transient thermal impedance

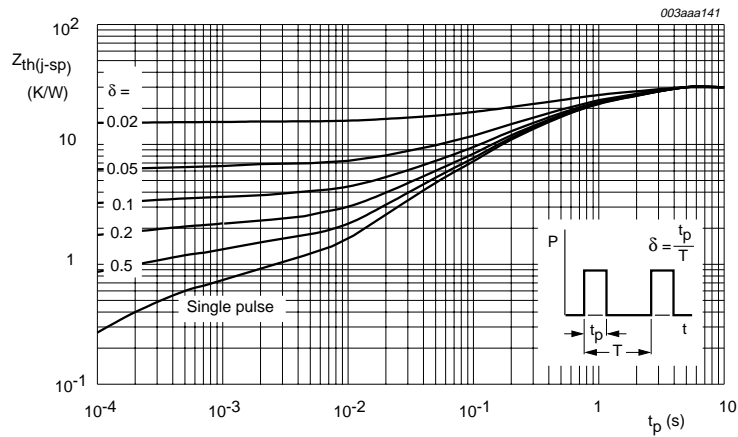


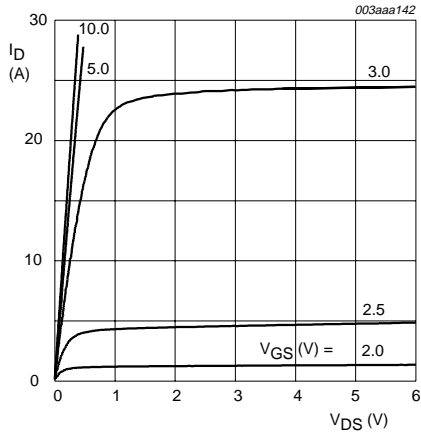
Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration.

8. Characteristics

Table 5: Characteristics

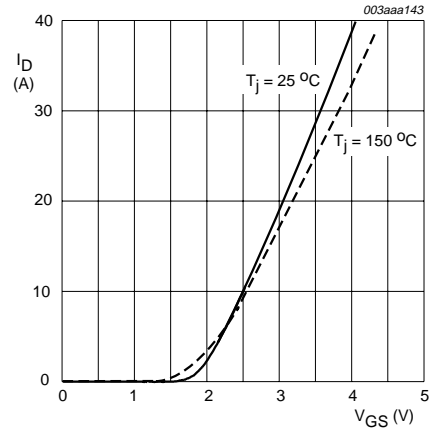
$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$	20	–	–	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 200\text{ }\mu\text{A}$; $V_{DS} = 10\text{ V}$; Figure 9	0.5	–	1.5	V
I_{DSS}	drain-source leakage current	$V_{DS} = 20\text{ V}$; $V_{GS} = 0\text{ V}$ $T_j = 25\text{ }^\circ\text{C}$ $T_j = 150\text{ }^\circ\text{C}$	–	0.05	10	μA
			–	–	500	μA
			–	–	–	–
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 12\text{ V}$; $V_{DS} = 0\text{ V}$	–	–	± 1	μA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 3\text{ A}$; Figure 7 and 8 $T_j = 25\text{ }^\circ\text{C}$ $T_j = 150\text{ }^\circ\text{C}$ $V_{GS} = 2.5\text{ V}$; $I_D = 3\text{ A}$	–	16	20	$\text{m}\Omega$
			–	–	30	$\text{m}\Omega$
			–	36	45	$\text{m}\Omega$
Dynamic characteristics						
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}$; $I_D = 3\text{ A}$;	8.5	11	–	S
$Q_{g(tot)}$	total gate charge	$I_D = 6\text{ A}$; $V_{DD} = 16\text{ V}$; $V_{GS} = 5\text{ V}$; Figure 13	–	20	–	nC
Q_{gs}	gate-source charge		–	4	–	nC
Q_{gd}	gate-drain (Miller) charge		–	10	–	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DD} = 10\text{ V}$; $f = 1\text{ MHz}$; Figure 11	–	910	–	pF
C_{oss}	output capacitance		–	600	–	pF
C_{rss}	reverse transfer capacitance		–	400	–	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 10\text{ V}$; $R_D = 3.3\text{ }\Omega$; $V_{GS} = 5\text{ V}$; $R_G = 4.7\text{ }\Omega$	–	11	–	ns
t_r	rise time		–	42	–	ns
$t_{d(off)}$	turn-off delay time		–	140	–	ns
t_f	fall time		–	96	–	ns
Source-drain (reverse) diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 6\text{ A}$; $V_{GS} = 0\text{ V}$; Figure 12	–	–	1.2	V



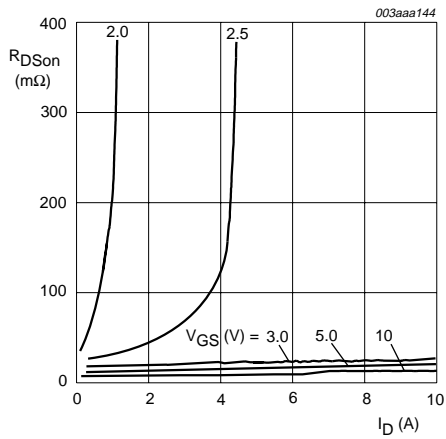
$T_j = 25\text{ }^\circ\text{C}$; $t_p = 300\text{ }\mu\text{s}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



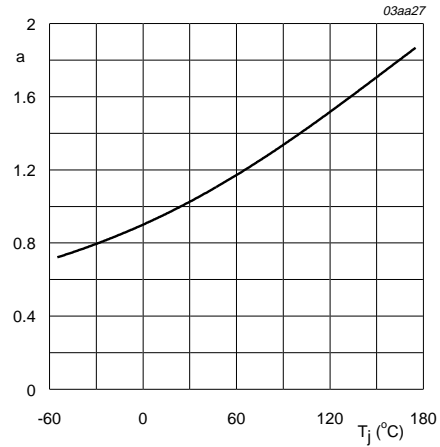
$V_{DS} = 10\text{ V}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



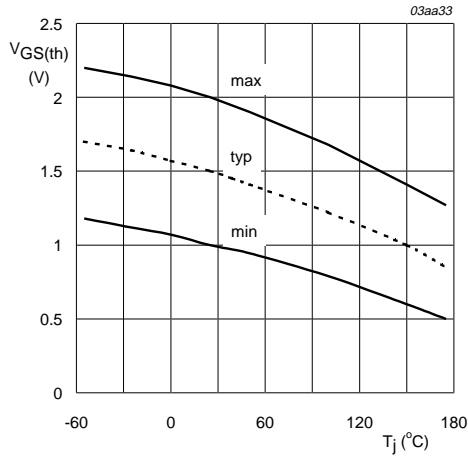
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



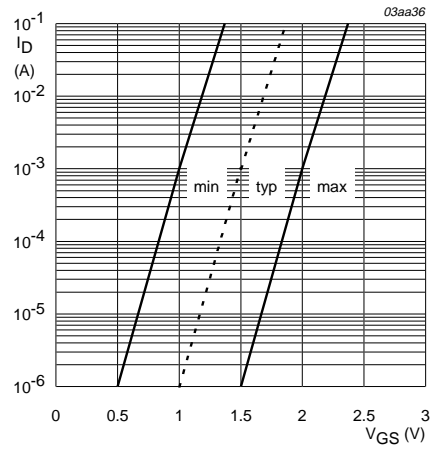
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



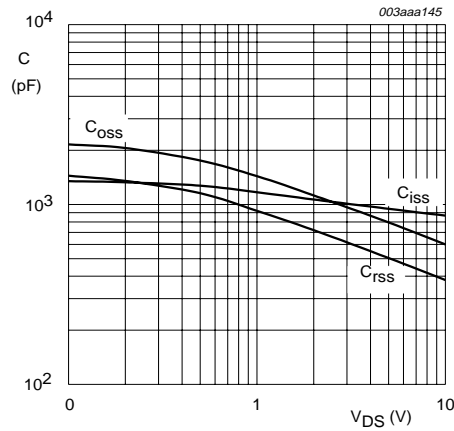
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



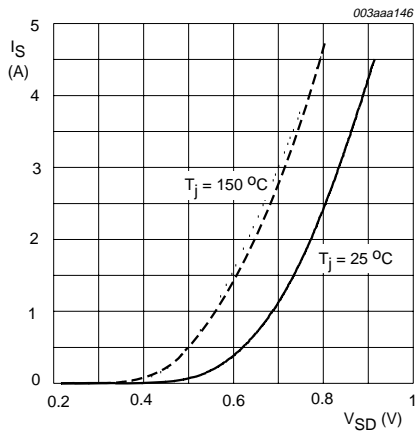
$T_j = 25 \text{ }^{\circ}C; V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



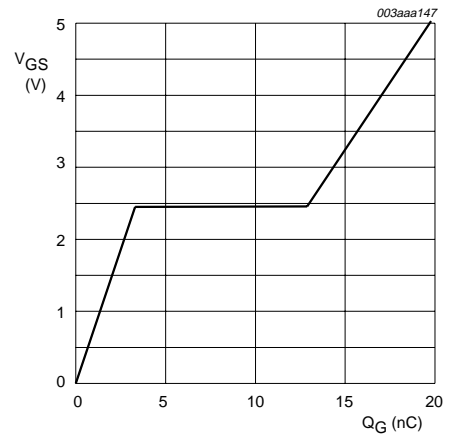
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$.

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{GS} = 0\text{ V}$

Fig 12. Reverse diode current as a function of reverse diode voltage; typical values.



$T_j = 25\text{ }^\circ\text{C}$; $I_D = 6\text{ A}$

Fig 13. Gate-source voltage as a function of turn-on gate charge; typical values.

9. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

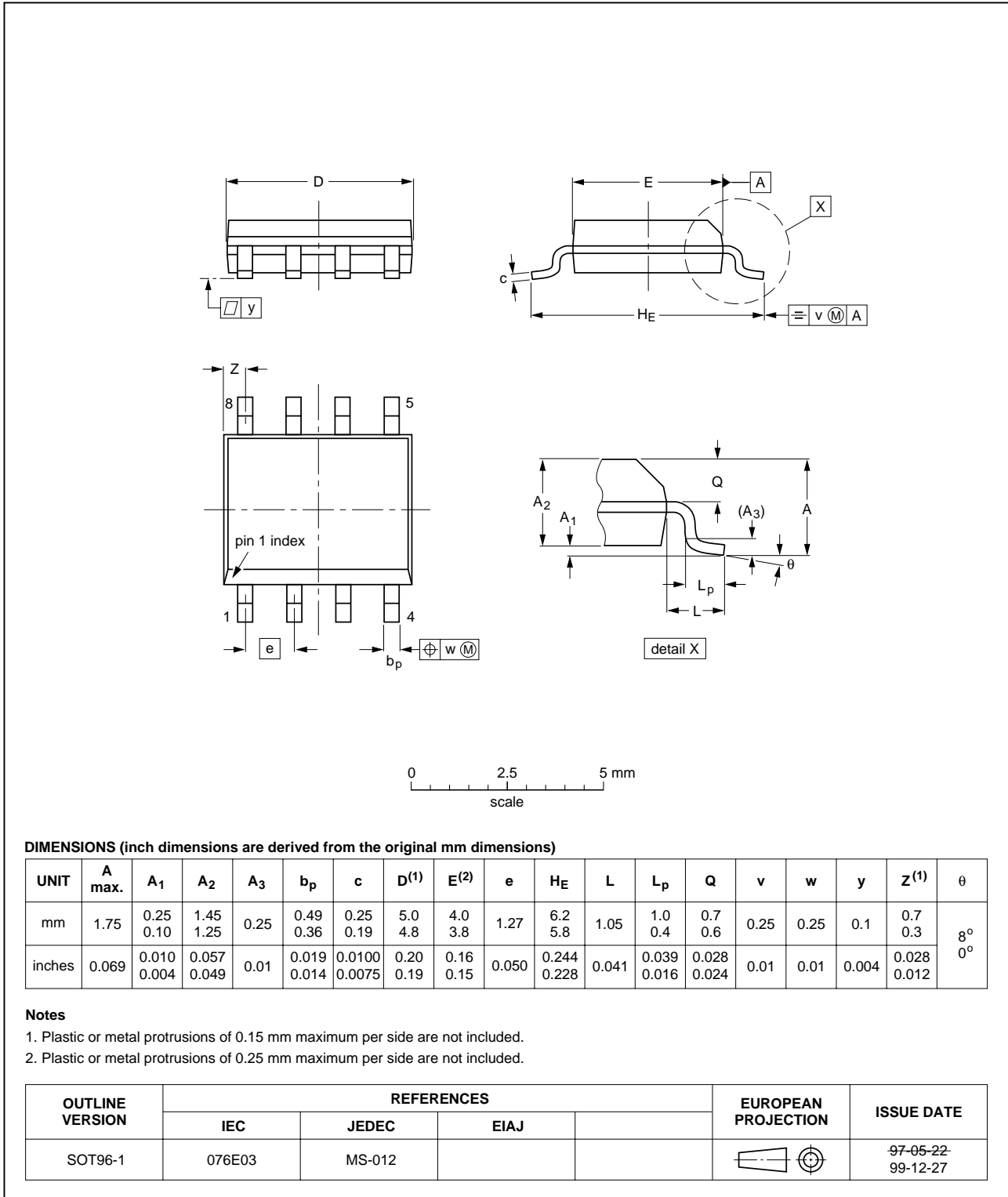


Fig 14. SOT96-1 (SO8).

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20010907	-	Product data; initial version

11. Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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