

LINEAR SYSTEMS

Linear Integrated Systems

ID100 ID101

**MONOLITHIC DUAL
PICO AMPERE DIODES**

FEATURES

DIRECT REPLACEMENT FOR INTERSIL ID100 & ID101

REVERSE LEAKAGE CURRENT $I_R = 0.1\text{pA}$

REVERSE BREAKDOWN VOLTAGE $BV_R \geq 30\text{V}$

REVERSE CAPACITANCE $C_{RSS} = 0.75\text{pF}$

ABSOLUTE MAXIMUM RATINGS¹

@ 25 °C (unless otherwise stated)

Maximum Temperatures

Storage Temperature -65 to +200 °C

Operating Junction Temperature -55 to +150 °C

Maximum Power Dissipation

Continuous Power Dissipation 300mW

Maximum Currents

Forward Current 20mA

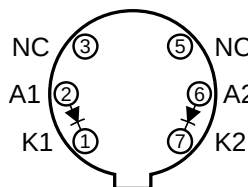
Reverse Current 100μA

Maximum Voltages

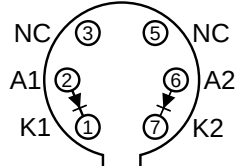
Reverse Voltage 30V

Diode to Diode Voltage ±50V

ID100
TO-78
BOTTOM VIEW



ID101
TO-71
BOTTOM VIEW



ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_R	Reverse Breakdown Voltage	30			V	$I_R = 1\mu\text{A}$
V_F	Forward Voltage	0.8		1.1		$I_F = 10\text{mA}$
I_R	Reverse Leakage Current		0.1		pA	$V_R = 1\text{V}$
			2.0	10		$V_R = 10\text{V}$
$ I_{R1} - I_{R2} $	Differential Leakage Current			3		
C_{RSS}	Total Reverse Capacitance ²		0.75	1	pF	$V_R = 10\text{V}, f = 1\text{MHz}$

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Figure 1. Operational Amplifier Protection

Input Differential Voltage limited to 0.8V (typ) by Diodes ID100 D₁ and D₂.
Common Mode Input voltage limited by Diodes ID100 D₃ and D₄ to $\pm 15V$.

Figure 2. Sample and Hold Circuit

Typical Sample and Hold circuit with clipping. ID100 diodes reduce offset voltages fed capacitively from the ID100 switch gate.

FIGURE 1

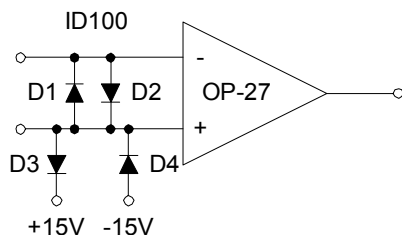
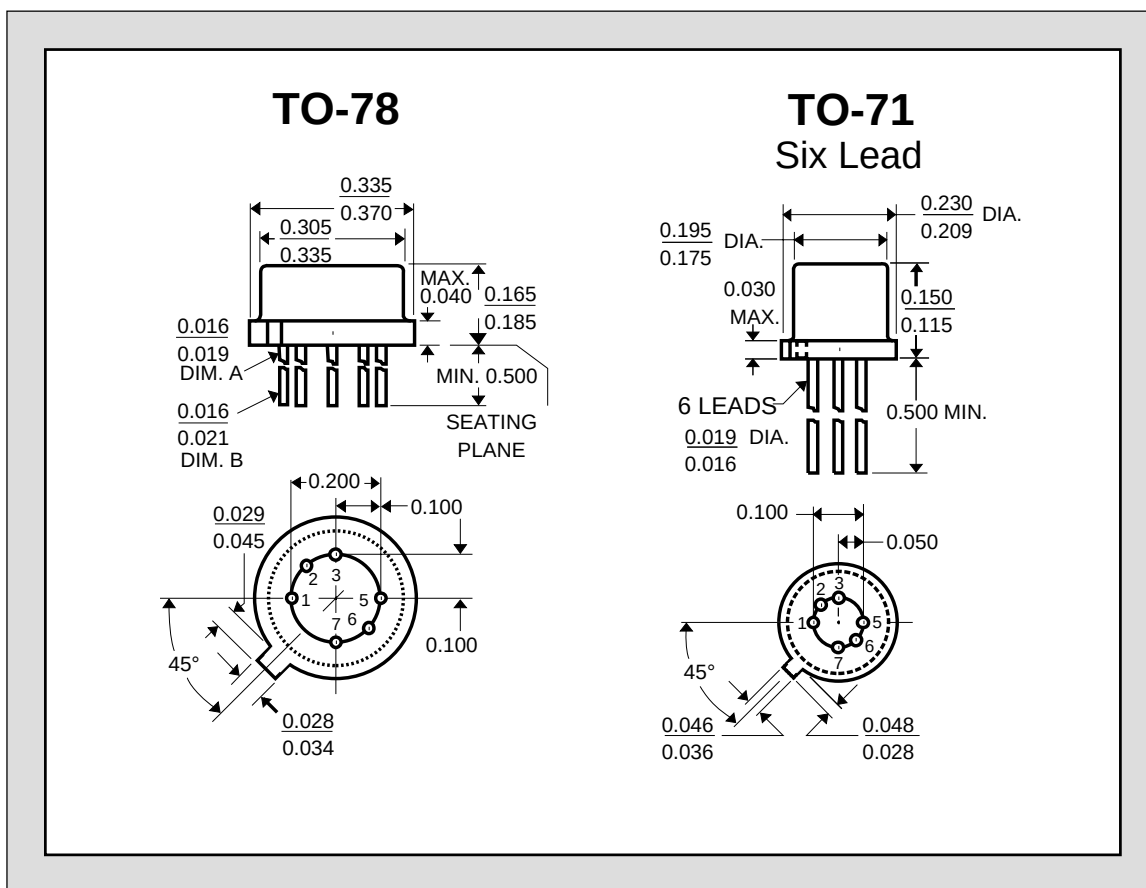
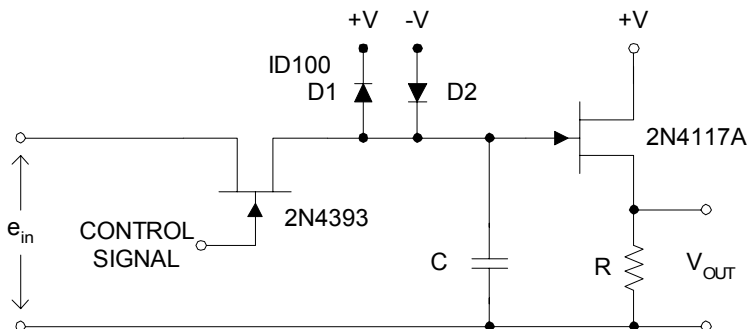


FIGURE 2



1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Design reference only, not 100% tested.
3. Pins 3 & 5 on ID100 and ID101 must not be connected, in any fashion or manner, to any circuit or node.

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