

2-INPUT AND GATE

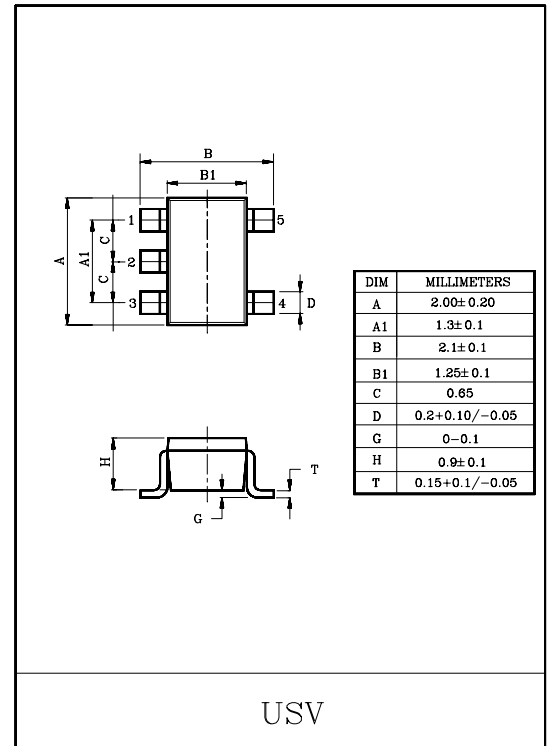
The KIC7SH08FU is a advanced high speed CMOS-2 INPUT AND GATE fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The internal circuit is composed of 4 stage including buffer output, which provide high noise immunity and stable output. An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interfase 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES

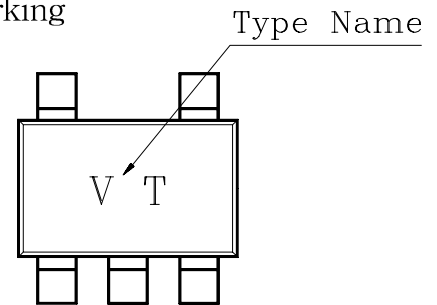
- High Speed : $t_{pd}=4.3ns$ (Typ.) at $V_{CC}=5V$.
- Low Power Dissipation : $I_{CC}=2\mu A$ (Max.) at $T_a=25^{\circ}C$.
- High Noise Immunity : $V_{NIH}=V_{NIL}=28\% V_{CC}$ (Min.).
- Power Down Protection is Provided on all inputs.
- Balanced Propagation Delays : $t_{pLH}\approx t_{pHL}$
- Wide Operating Voltage Range : $V_{CC(opr)}=2\sim 5.5V$.

MAXIMUM RATINGS ($T_a=25^{\circ}C$)

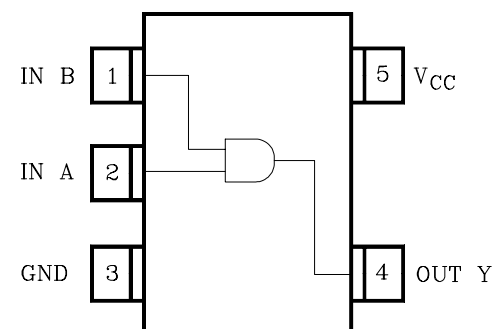
CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage	V_{IN}	-0.5~7.0	V
DC Output Voltage	V_{OUT}	-0.5~ $V_{CC}+0.5$	V
Input Diode Current	I_{IK}	-20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} /Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	200	mW
Storage Temperature	T_{stg}	-65~150	$^{\circ}C$
Lead Temperature (10s)	T_L	260	$^{\circ}C$



Marking

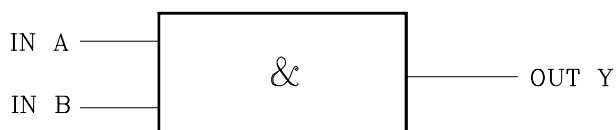


PIN CONNECTION(TOP VIEW)



KIC7SH08FU

LOGIC DIAGRAM



TRUTH TABLE

A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	t_r, t_f	0~100 ($V_{CC}=3.3\pm 0.3V$)	ns/V
		0~20 ($V_{CC}=5\pm 0.5V$)	

DC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITION		$T_a=25^\circ C$			$T_a=-40\sim 85^\circ C$		UNIT	
				V_{CC}	MIN.	TYP.	MAX.	MIN.		MAX.
High-Level Input Voltage	V_{IH}	-	-	2.0 3.0~ 5.5	1.50 V_{CC} $\times 0.7$	- - -	- - -	1.50 V_{CC} $\times 0.7$	- - -	V
Low-Level Input Voltage	V_{IL}	-	-	2.0 3.0~ 5.5	- -	- -	0.50 V_{CC} $\times 0.3$	- -	0.50 V_{CC} $\times 0.3$	V
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IL}$	$I_{OH}=-50\mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	- - -	1.9 2.9 4.4	- - -	V
		$V_{IN}=GND$	$I_{OH}=-4mA$ $I_{OH}=-8mA$	3.0 4.5	2.58 3.94	- -	- -	2.48 3.80	- -	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$	$I_{OL}=50\mu A$	2.0 3.0 4.5	- - -	0.0 0.0 0.0	0.1 0.1 0.1	- - -	0.1 0.1 0.1	V
		$V_{IN}=V_{CC}$	$I_{OL}=4mA$ $I_{OL}=8mA$	3.0 4.5	- -	- -	0.36 0.36	- -	0.44 0.44	
Input Leakage Current	I_{IN}	$V_{IN}=5.5V$ or GND		0~5.5	-	-	± 0.1	-	± 1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		5.5	-	-	2.0	-	20.0	

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AC ELECTRICAL CHARACTERISTICS (Input $t_r=t_f=3ns$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	Ta=25°C			Ta=-40~85°C		UNIT		
			V _{CC} (V)	C _L (pF)	MIN.	TYP.	MAX.		MIN.	MAX.
Propagation Delay Time	t _{PLH} t _{PHL}	-	3.3±0.3	15	-	6.2	8.8	1.0	10.5	ns
				50	-	8.7	12.3	1.0	14.0	
			5.0±0.5	15	-	4.3	5.9	1.0	7.0	
				50	-	5.8	7.9	1.0	9.0	
Input Capacitance	C _{IN}	-	-	4	10	-	10	pF		
Power Dissipation Capacitance	C _{PD}	(Note 1)	-	14	-	-	-			

Note 1 : C_{PD} defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load average operating current can be obtained by the equation hereunder.

$$I_{CC(oper)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

INPUT EQUIVALENT CIRCUIT

