

TC74HC595AP, TC74HC595AF, TC74HC595AFN**8 – BIT SHIFT REGISTER / LATCH (3 – STATE)**

The TC74HC595A is a high speed 8–BIT SHIFT REGISTER / LATCH fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. The TC74HC595A contains an 8–bit static shift register which feeds an 8–bit storage register.

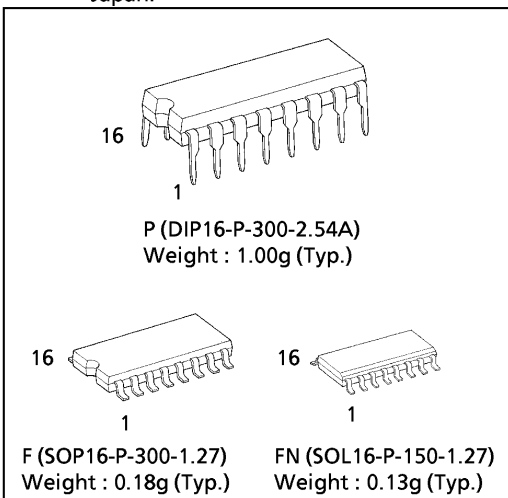
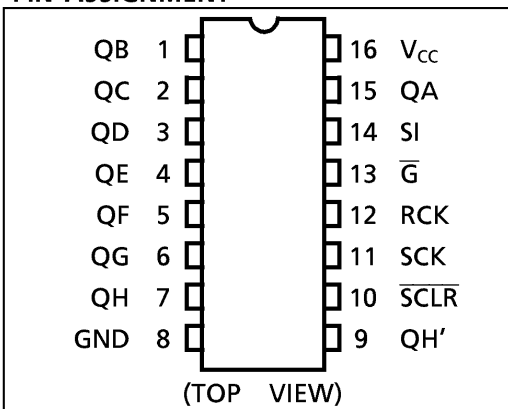
Shift operation is accomplished on the positive going transition of the SCK input. The output register is loaded with the contents of the shift register on the positive going transition of the RCK input. Since RCK and SCK signal are independent, parallel outputs can be held stable during the shift operation. And, since the parallel outputs are 3–state, it can be directly connected to 8–bit bus. This register can be used in serial–to–parallel conversion, data receivers, etc.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

- High Speed..... $f_{MAX} = 55\text{MHz}(\text{typ.})$
at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}(\text{Min.})$
- Output Drive Capability..... 15 LSTTL Loads For QA~QH
10 LSTTL Loads For QH'
- Symmetrical Output Impedance... $|I_{OH}| = |I_{OL}| = 6\text{mA}(\text{Min.})$
For QA~QH
 $|I_{OH}| = |I_{OL}| = 4\text{mA}(\text{Min.})$
For QH'
- Balanced Propagation Delays..... $t_{PLH} \approx t_{PHL}$
- Wide Operating Voltage Range.... $V_{CC}(\text{opr.}) = 2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 74LS595

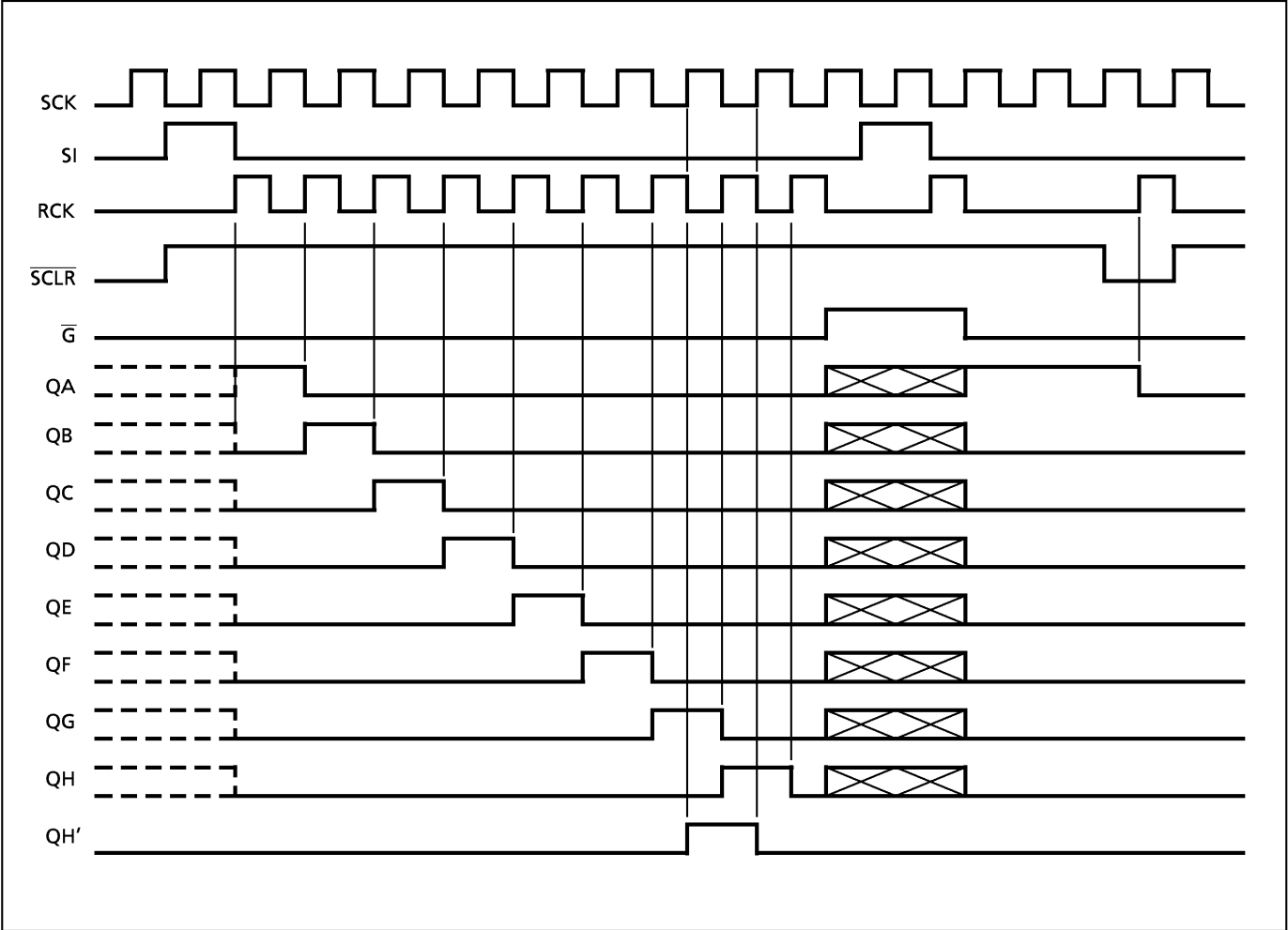
(Note) The JEDEC SOP (FN) is not available in Japan.

**PIN ASSIGNMENT****TRUTH TABLE**

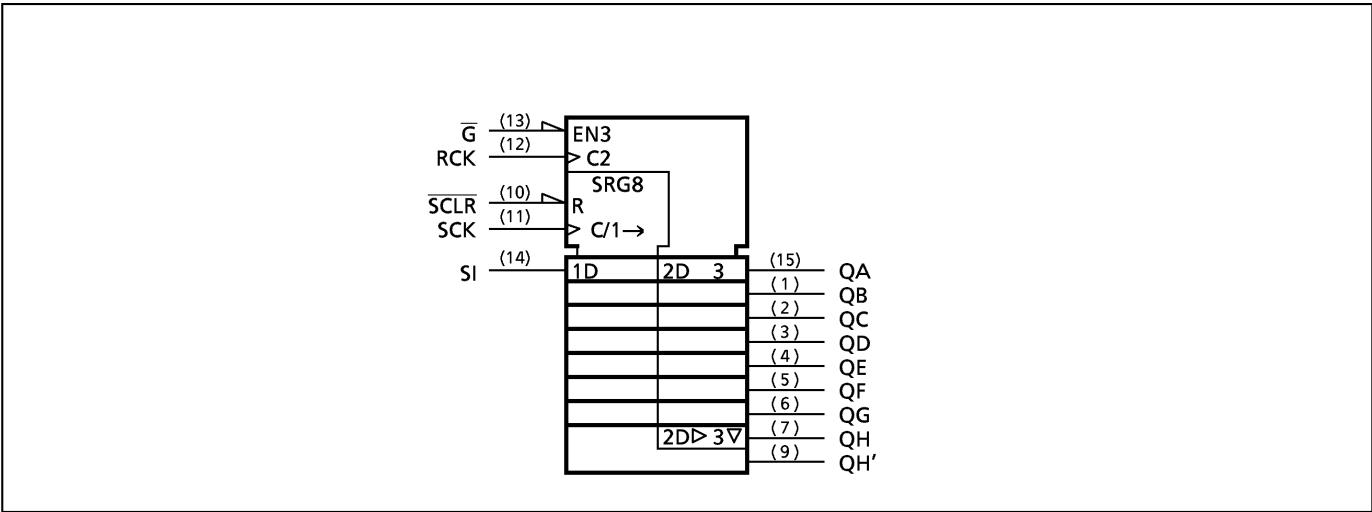
INPUTS					FUNCTION
SI	SCK	$\overline{\text{SCLR}}$	RCK	$\overline{\text{G}}$	
X	X	X	X	H	QA thru QH outputs disable
X	X	X	X	L	QA thru QH outputs enable
X	X	L	X	X	Shift register is cleared.
L		H	X	X	First stage of S. R. becomes "L". Other stages store the data of previous stage, respectively.
H		H	X	X	First stage of S. R. becomes "H". Other stages store the data of previous stage, respectively.
X		H	X	X	State of S. R. is not changed.
X	X	X		X	S.R. data is stored into storage register.
X	X	X		X	Storage register stage is not changed.

X : Don't Care

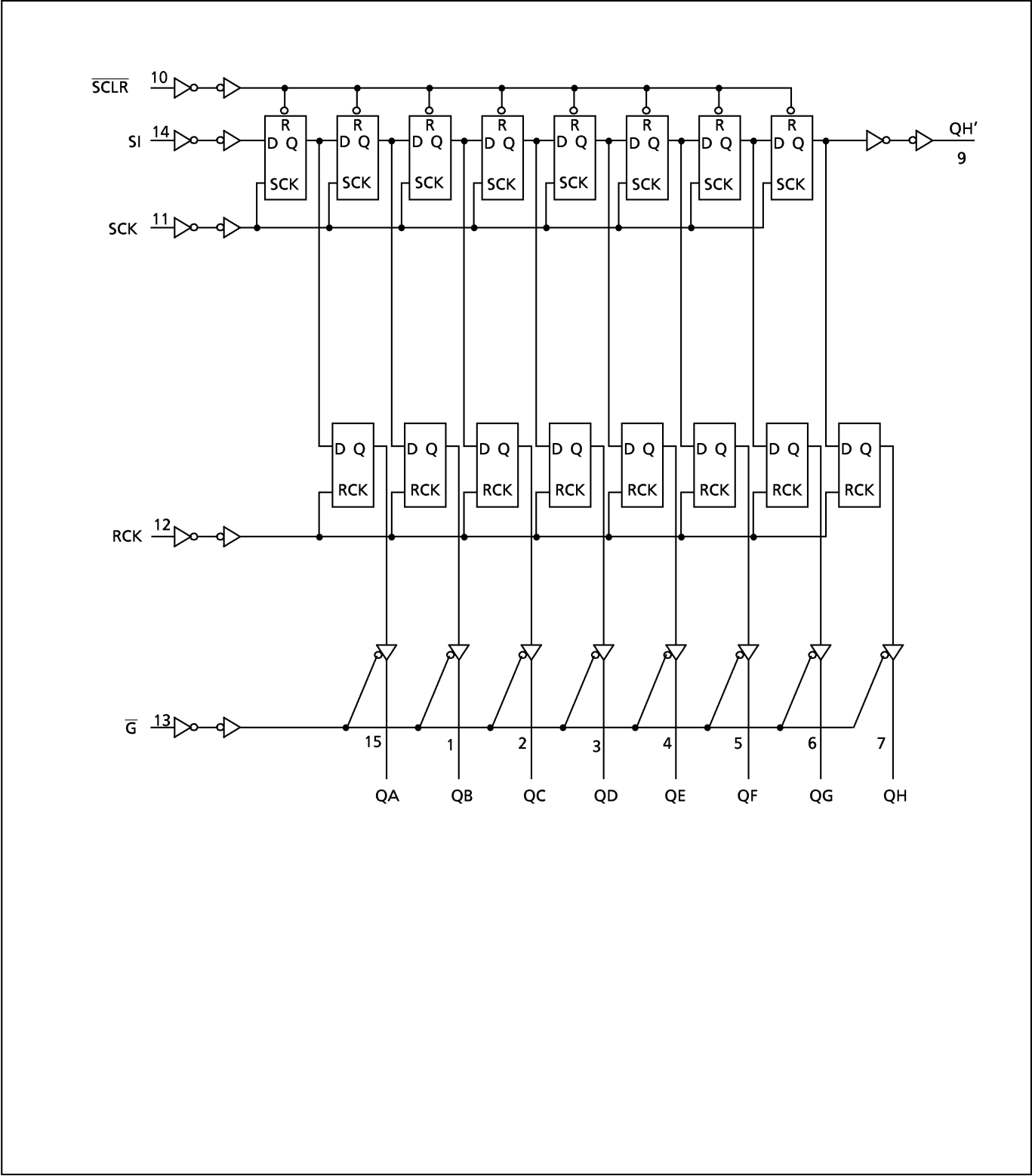
TIMING CHART



IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current (QH') (QA~QH)	I_{OUT}	± 25 ± 35	mA
DC V_{CC} /Ground Current	I_{CC}	± 75	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C

*500mW in the range of $T_a = -40^\circ\text{C} \sim 65^\circ\text{C}$. From $T_a = 65^\circ\text{C}$ to 85°C a derating factor of $-10\text{mW}/^\circ\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$ ($V_{CC} = 2.0\text{V}$) $0 \sim 500$ ($V_{CC} = 4.5\text{V}$) $0 \sim 400$ ($V_{CC} = 6.0\text{V}$)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Input Voltage	V_{IL}		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -20\mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	V
		QH'	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —	
		QA~QH	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 20\mu\text{A}$	2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
		QH'	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
		QA~QH	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
3 - State Output Off - State Current	I_{OZ}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = V_{CC} \text{ or GND}$	6.0	—	—	± 0.5	—	± 5.0	μA
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC} \text{ or GND}$	6.0	—	—	± 0.1	—	± 1.0	
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC} \text{ or GND}$	6.0	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C		Ta = -40~85°C	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (SCK, RCK)	$t_{W(H)}$ $t_{W(L)}$		2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Pulse Width ($\overline{\text{SCLR}}$)	$t_{W(L)}$		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set-up Time (SI—SCK)	t_s		2.0	—	50	65	
			4.5	—	10	13	
			6.0	—	9	11	
Minimum Set-up Time (SCK—RCK)	t_s		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set-up Time ($\overline{\text{SCLR}}$ —RCK)	t_s		2.0	—	100	125	
			4.5	—	20	25	
			6.0	—	17	21	
Minimum Hold Time	t_h		2.0	—	0	0	
			4.5	—	0	0	
			6.0	—	0	0	
Minimum Removal Time ($\overline{\text{SCLR}}$)	t_{rem}		2.0	—	50	65	
			4.5	—	10	13	
			6.0	—	9	11	
Clock Frequency	f		2.0	—	6	5	MHz
			4.5	—	30	25	
			6.0	—	35	28	

AC ELECTRICAL CHARACTERISTICS ($C_L = 15\text{pF}$, $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time (QH')	t_{TLH} t_{THL}		—	4	8	ns
Propagation Delay Time (SCK—QH')	t_{pLH} t_{pHL}		—	12	21	
Propagation Delay Time (SCLR—QH')	t_{pHL}		—	15	30	
Maximum Clock Frequency	f_{MAX}		35	77	—	MHz

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	CL (pF)	V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time (Q _n)	t_{TLH} t_{THL}		50	2.0 4.5 6.0	— — —	25 7 6	60 12 10	— — —	75 15 13	ns
Output Transition Time (QH')	t_{TLH} t_{THL}		50	2.0 4.5 6.0	— — —	30 8 7	75 15 13	— — —	95 19 16	
Propagation Delay Time (SCK—QH')	t_{pLH} t_{pHL}		50	2.0 4.5 6.0	— — —	45 15 13	125 25 21	— — —	155 31 26	
Propagation Delay Time (SCLR—QH')	t_{pHL}		50	2.0 4.5 6.0	— — —	60 18 15	175 35 30	— — —	220 44 37	
Propagation Delay Time (RCK—Q _n)	t_{pLH} t_{pHL}		50	2.0	—	60	150	—	190	
				4.5	—	20	30	—	38	
				6.0	—	17	26	—	32	
			150	2.0	—	75	190	—	240	
				4.5	—	25	38	—	48	
				6.0	—	22	32	—	41	
Output Enable time	t_{pZL} t_{pZH}	R _L = 1kΩ	50	2.0	—	45	135	—	170	
				4.5	—	15	27	—	34	
				6.0	—	13	23	—	29	
			150	2.0	—	60	175	—	220	
				4.5	—	20	35	—	44	
				6.0	—	17	30	—	37	
Output Disable time	t_{pLZ} t_{pHZ}	R _L = 1kΩ	50	2.0	—	30	150	—	190	
				4.5	—	15	30	—	38	
				6.0	—	14	26	—	33	
Maximum Clock Frequency	f_{MAX}		50	2.0 4.5 6.0	6 30 35	17 50 59	— — —	5 25 28	— — —	MHz
Input Capacitance	C_{IN}				—	5	10	—	10	pF
Power Dissipation Capacitance	$C_{PD}(1)$				—	184	—	—	—	

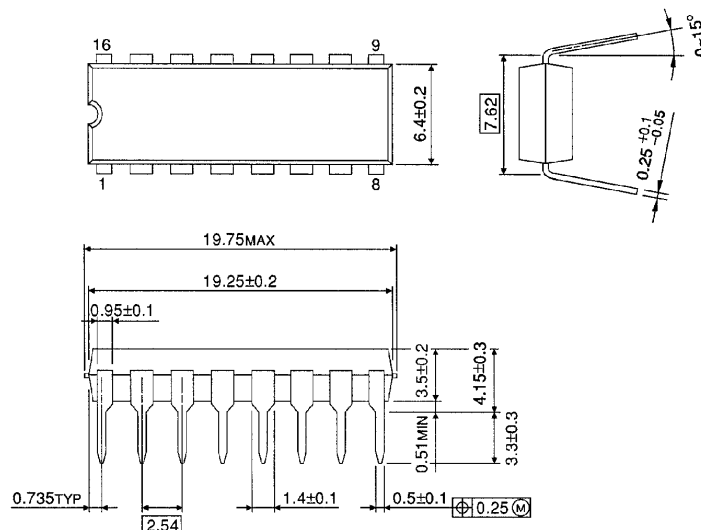
Note(1): C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

DIP 16PIN PACKAGE DIMENSIONS (DIP16-P-300-2.54A)

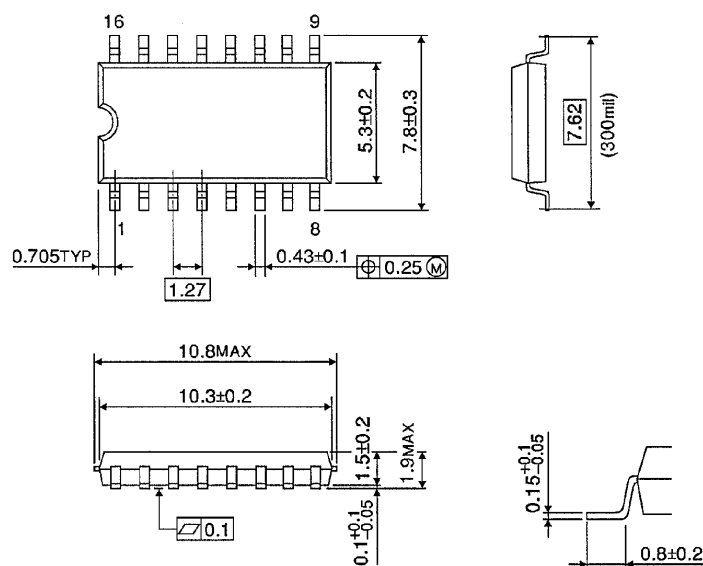
Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27)

Unit in mm

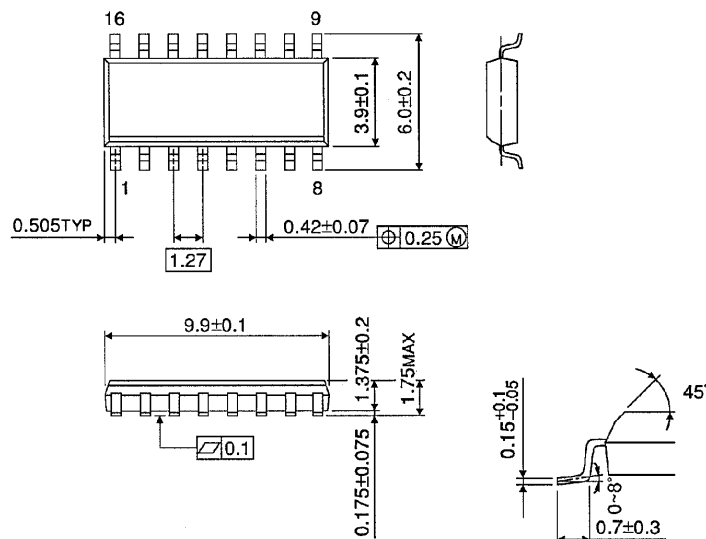


Weight : 0.18g (Typ.)

SOP 16PIN (150mil BODY) PACKAGE DIMENSIONS (SOL16-P-150 -1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)

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