

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HC597AP, TC74HC597AF

8-BIT LATCH/SHIFT REGISTER

The TC74HC597A is a high speed CMOS 8-BIT PARALLEL-IN/SERIAL-IN SERIAL-OUT LATCH/SHIFT REGISTER fabricated with silicon gate CMOS technology.

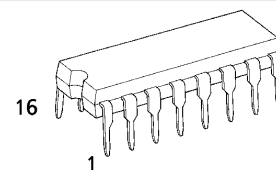
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It consists of an 8-bit data register feeding an 8-bit shift register. The parallel data on the A~H inputs is stored in the input register on the positive going transition of RCK. When the $\overline{\text{SLOAD}}$ input is held low, the input register data is passed into the shift registers. When $\overline{\text{SLOAD}}$ input is held high, the serial data input (SI) is enabled and the eight flip-flops perform serial shifting on the positive transition of SCK. A direct clear input ($\overline{\text{SCLR}}$) sets the 8-bit shift register to zero.

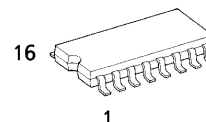
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed..... $f_{\text{MAX}} = 60\text{MHz}$ (typ.)
at $V_{\text{CC}} = 5\text{V}$
- Low Power Dissipation..... $I_{\text{CC}} = 4\mu\text{A}$ (Max.) at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{\text{NIH}} = V_{\text{NIL}} = 28\%V_{\text{CC}}$
- Output Drive Capability..... 10 LSTTL Loads
- Symmetrical Output Impedance... $|I_{\text{OH}}| = |I_{\text{OL}}| = 4\text{mA}$ (Min.)
- Balanced Propagation Delays..... $t_{\text{PLH}} \approx t_{\text{PHL}}$
- Wide Operating Voltage Range... $V_{\text{CC}} (\text{opr.}) = 2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 74LS597

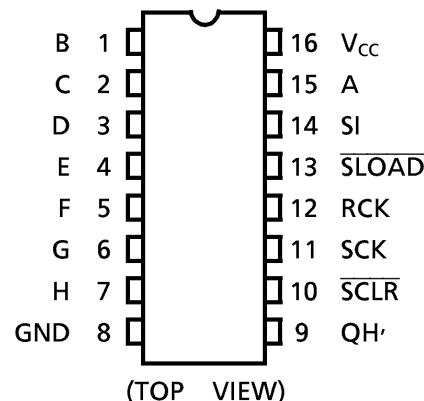


P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)



F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)

PIN ASSIGNMENT

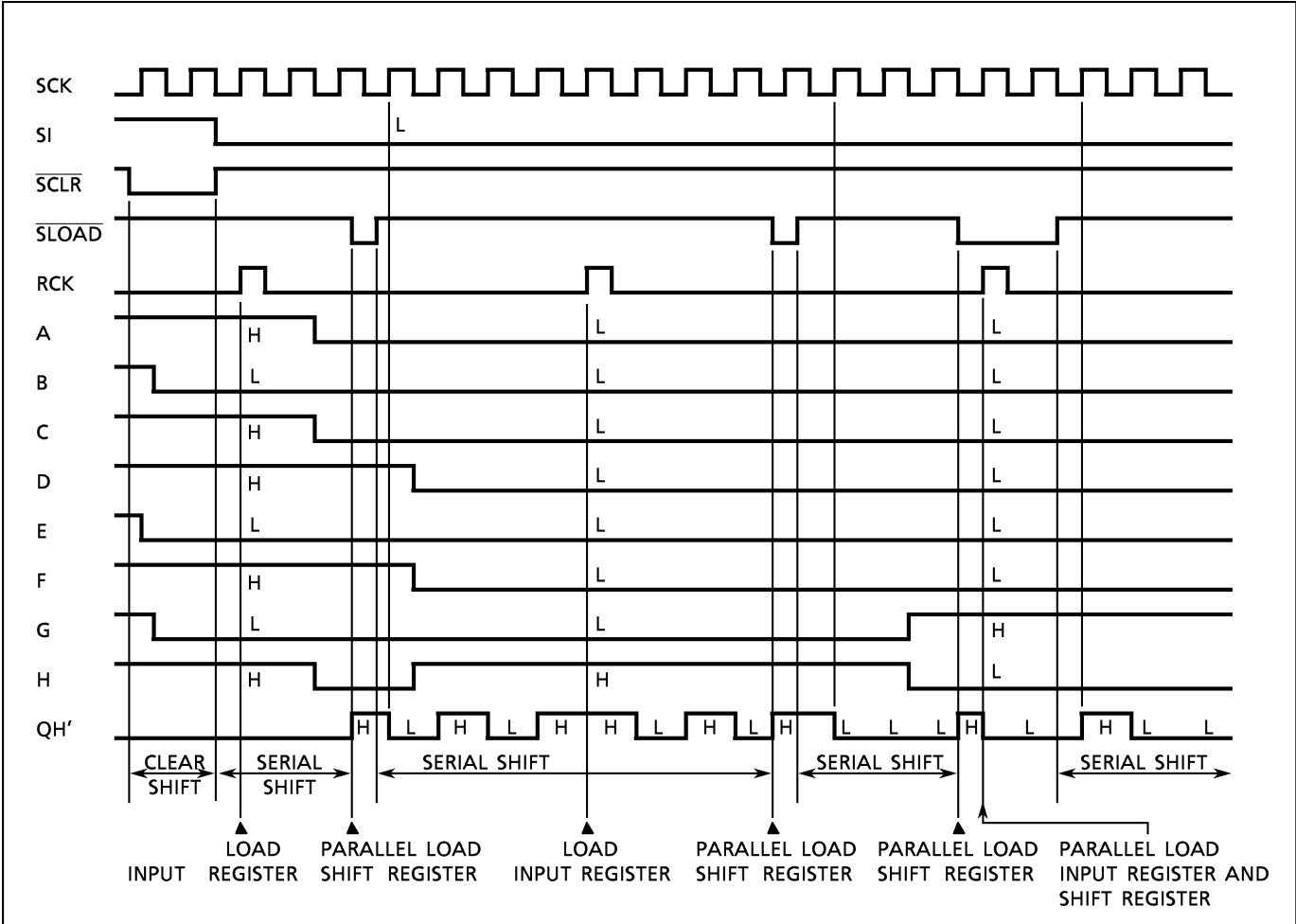


TRUTH TABLE

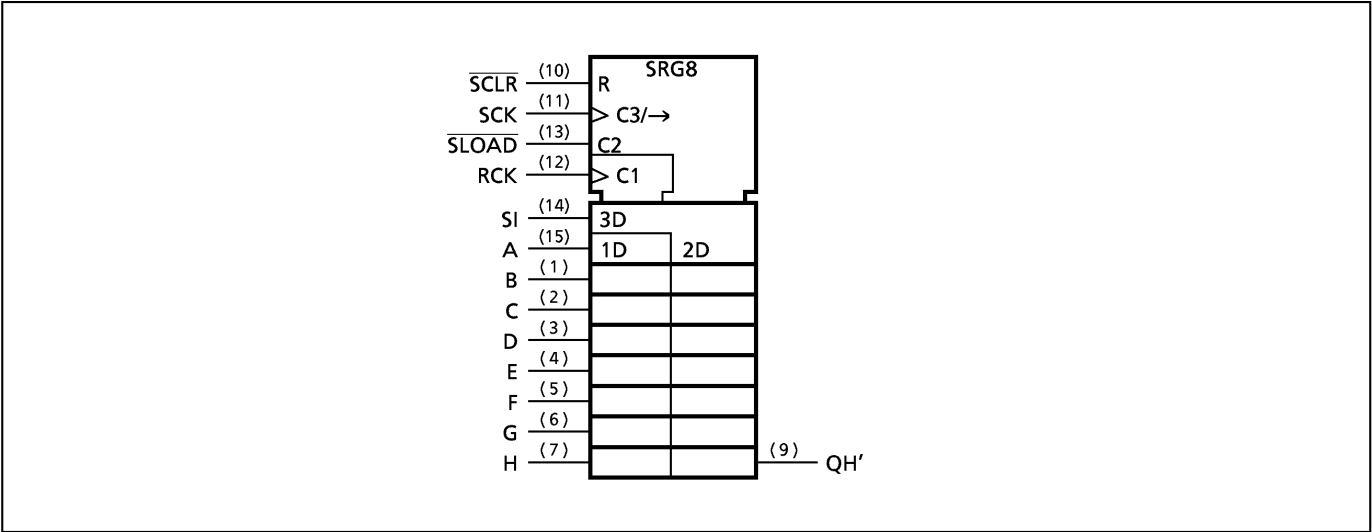
INPUTS					FUNCTION
SI	SCK	$\overline{\text{SCLR}}$	$\overline{\text{SLOAD}}$	RCK	
X	X	L	H	X	S. R. is cleared to "L"
X	X	H	L	X	Input register data is stored into S. R.
L		H	H	X	First stage of S. R. become "L". Other stages store the data of previous stage, respectively.
H		H	H	X	First stage of S. R. become "H". Other stages store the data of previous stage, respectively.
X		H	H	X	State of S. R. is not changed.
X	X	X	X		Input data on A~H line is stored into input register.
X	X	X	X		Storage register stage is not changed.

X : Don't Care

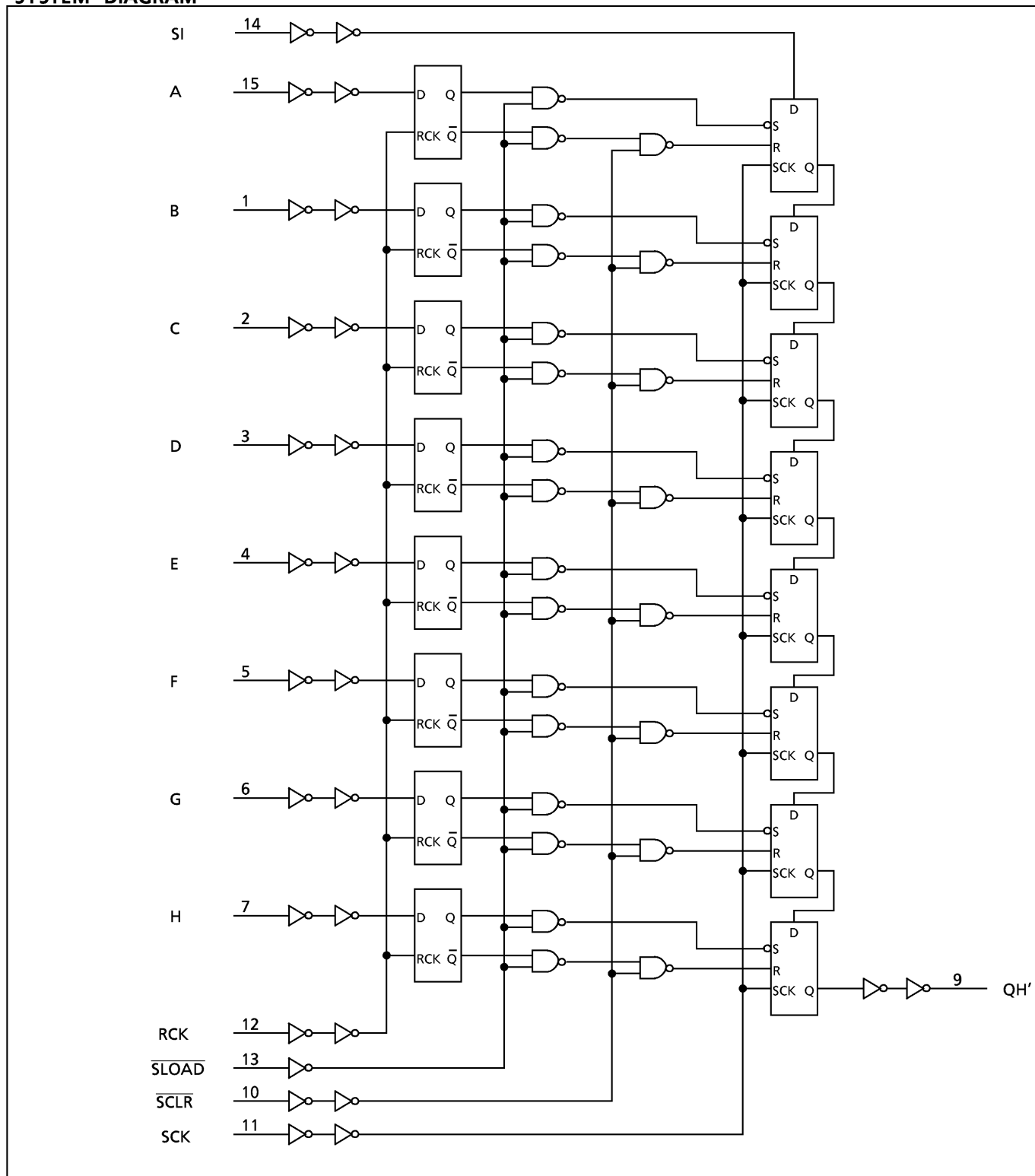
TIMING CHART



IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7.0$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} /Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C

*500mW in the range of $T_a = -40^\circ\text{C} \sim 65^\circ\text{C}$. From $T_a = 65^\circ\text{C}$ to 85°C a derating factor of $-10\text{mW}/^\circ\text{C}$ should be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~ V_{CC}	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	t_r, t_f	0~1000 ($V_{CC} = 2.0\text{V}$) 0~500 ($V_{CC} = 4.5\text{V}$) 0~400 ($V_{CC} = 6.0\text{V}$)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}		2.0	1.50	—	—	1.50	—	V
			4.5	3.15	—	—	3.15	—	
			6.0	4.20	—	—	4.20	—	
Low - Level Input Voltage	V_{IL}		2.0	—	—	0.50	—	0.50	V
			4.5	—	—	1.35	—	1.35	
			6.0	—	—	1.80	—	1.80	
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20\mu\text{A}$	2.0	1.9	2.0	—	1.9	V
				4.5	4.4	4.5	—	4.4	
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -4 \text{ mA}$ $I_{OH} = -5.2 \text{ mA}$	4.5	4.18	4.31	—	4.13	
				6.0	5.68	5.80	—	5.63	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20\mu\text{A}$	2.0	—	0.0	0.1	—	V
				4.5	—	0.0	0.1	—	
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 4 \text{ mA}$ $I_{OL} = 5.2 \text{ mA}$	4.5	—	0.17	0.26	—	
				6.0	—	0.18	0.26	—	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC} \text{ or GND}$	6.0	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC} \text{ or GND}$	6.0	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		Ta = -40~85°C		UNIT
			V _{CC} (V)	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (SCK, RCK)	$t_{W(H)}$ $t_{W(L)}$		2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Pulse Width (SCLR)	$t_{W(L)}$		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Pulse Width (SLOAD)	$t_{W(L)}$		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set-up Time (RCK—SLOAD)	t_s		2.0	—	100	125	
			4.5	—	20	25	
			6.0	—	17	21	
Minimum Set-up Time (SI—SCK)	t_s		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set-up Time (PI—RCK)	t_s		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Hold Time	t_h		2.0	—	0	0	
			4.5	—	0	0	
			6.0	—	0	0	
Minimum Removal Time (SCLR, SLOAD)	t_{rem}		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Clock Frequency	f		2.0	—	6	5	MHz
			4.5	—	30	24	
			6.0	—	35	28	

AC ELECTRICAL CHARACTERISTICS (C_L = 15pF, V_{CC} = 5V, Ta = 25°C, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		—	5	8	ns
Propagation Delay Time (SCK—QH')	t_{pLH} t_{pHL}		—	16	25	
Propagation Delay Time (SCLR—QH')	t_{pHL}		—	20	32	
Propagation Delay Time (SLOAD—QH')	t_{pLH} t_{pHL}		—	18	30	
Propagation Delay Time (RCK—QH')	t_{pLH} t_{pHL}	$\overline{\text{SLOAD}} = \text{“L”}$	—	25	37	
Clock Frequency	f_{MAX}		30	59	—	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}(\text{V})$	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	—	32	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation Delay Time ($\text{SCK} - \text{QH}'$)	t_{PLH} t_{PHL}		2.0	—	78	145	—	180	
			4.5	—	20	29	—	36	
			6.0	—	16	25	—	31	
Propagation Delay Time ($\text{SCLR} - \text{QH}'$)	t_{PHL}		2.0	—	90	175	—	220	
			4.5	—	24	35	—	44	
			6.0	—	20	30	—	37	
Propagation Delay Time ($\text{SLOAD} - \text{QH}'$)	t_{PLH} t_{PHL}		2.0	—	80	175	—	220	
			4.5	—	22	35	—	44	
			6.0	—	18	30	—	37	
Propagation Delay Time ($\text{RCK} - \text{QH}'$)	t_{PLH} t_{PHL}	$\text{SLOAD} = "L"$	2.0	—	112	210	—	265	ns
			4.5	—	30	42	—	53	
			6.0	—	24	36	—	45	
Maximum Clock Frequency	f_{MAX}		2.0	6	12	—	5	—	MHz
			4.5	30	48	—	24	—	
			6.0	35	50	—	28	—	
Input Capacitance	C_{IN}			—	5	10	—	10	pF
Power Dissipation Capacitance	$C_{PD} (1)$			—	60	—	—	—	

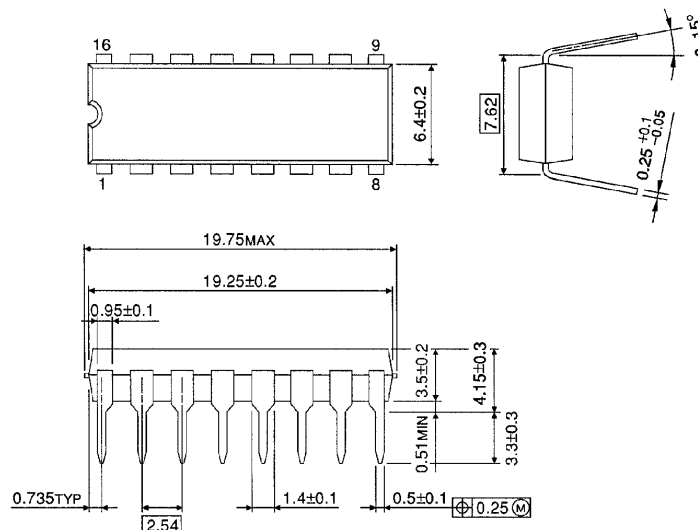
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

DIP 16PIN PACKAGE DIMENSIONS (DIP16-P-300-2.54A)

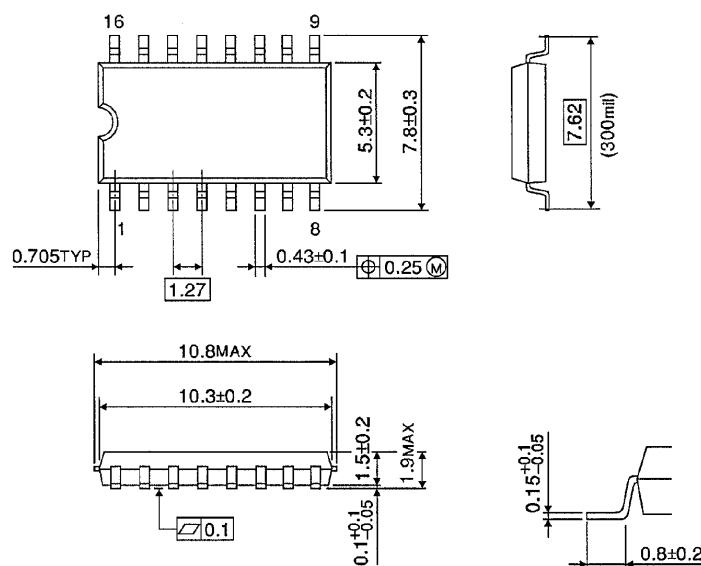
Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27)

Unit in mm



Weight : 0.18g (Typ.)

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