

TC74HC670AP, TC74HC670AF

4 WORD×4 BIT REGISTER FILE (3 – STATE)

The TC74HC670A is a high speed 4–WORD_S×4–BIT_S REGISTER FILE fabricated with silicon gate C2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The register file is organized as 4 words of 4 bits each.

Separate read and write address inputs (RA, RB, and WA, WB) and enable inputs ($\overline{RE}$, $\overline{WE}$) are available permitting simultaneous writing into one word location and reading from another location.

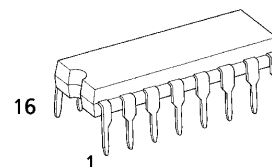
Four data inputs (D0~D3) are provided to store the 4-bit words.

The write address inputs (WA, WB) determine the location of the stored word in the register. When write Enable($\overline{WE}$) is held low, the data is entered into addressed location. When $\overline{WE}$ is held high, data and address inputs are inhibited. The data acquisition from the four registers is made possible by the read address inputs (RA, RB) when the Read Enable ($\overline{RE}$) is held low. When RE is held high the data outputs are in the high impedance state.

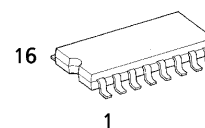
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed..... $t_{pd} = 23\text{ns}$ (Typ.)
at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}$ (Max.) at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance... $|I_{OH}| = I_{OL} = 4\text{mA}$ (Min.)
- Balanced Propagation Delays..... $t_{PLH} \approx t_{PHL}$
- Wide Operating Voltage Range... V_{CC} (opr.) = 2V~6V
- Pin and Function Compatible with 74LS670

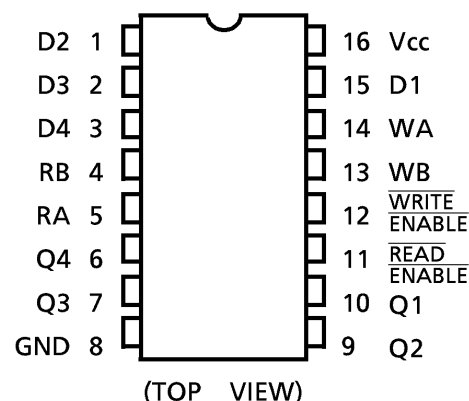


P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)

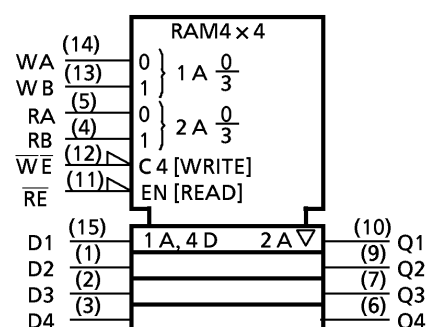


F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)

PIN ASSIGNMENT



IEC LOGIC SYMBOL



TRUTH TABLE

WRITE FUNCTION TABLE							READ FUNCTION TABLE						
WRITE INPUTS			WORDS				READ INPUTS			OUTPUTS			
WB	WA	WE	0	1	2	3	RB	RA	RE	Q1	Q2	Q3	Q4
L	L	L	Q = D	Q0	Q0	Q0	L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	Q0	Q = D	Q0	Q0	L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	Q0	Q0	Q = D	Q0	H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	Q0	Q0	Q0	Q = D	H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Q0	Q0	Q0	Q0	X	X	H	Z	Z	Z	Z

NOTES

1. X : Don't Care

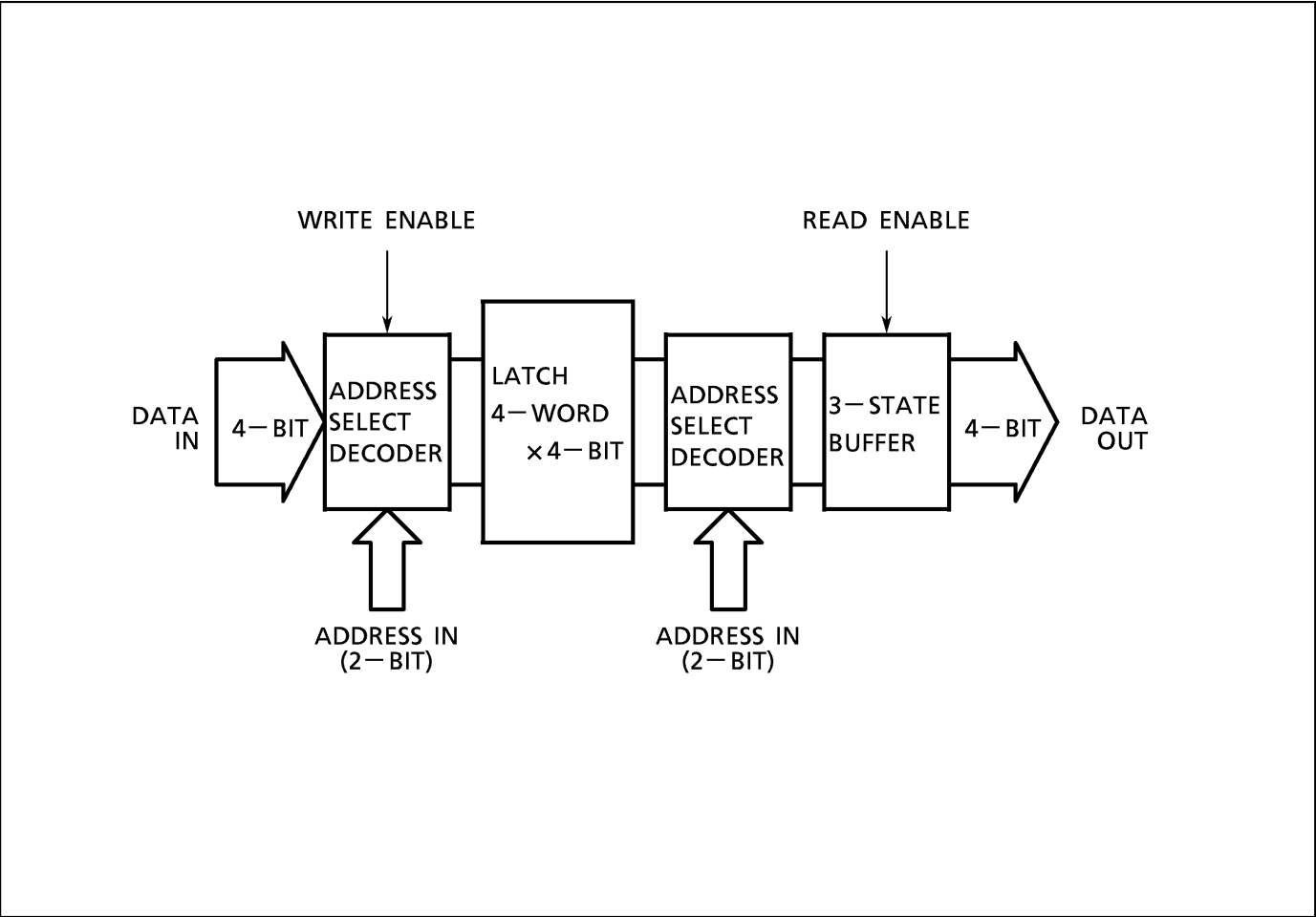
2. (Q = D) : The four selected internal flip-flop outputs will assume the states applied to the four external data Inputs.

3. Q0 : The level of Q before the indicated input conditions were established.

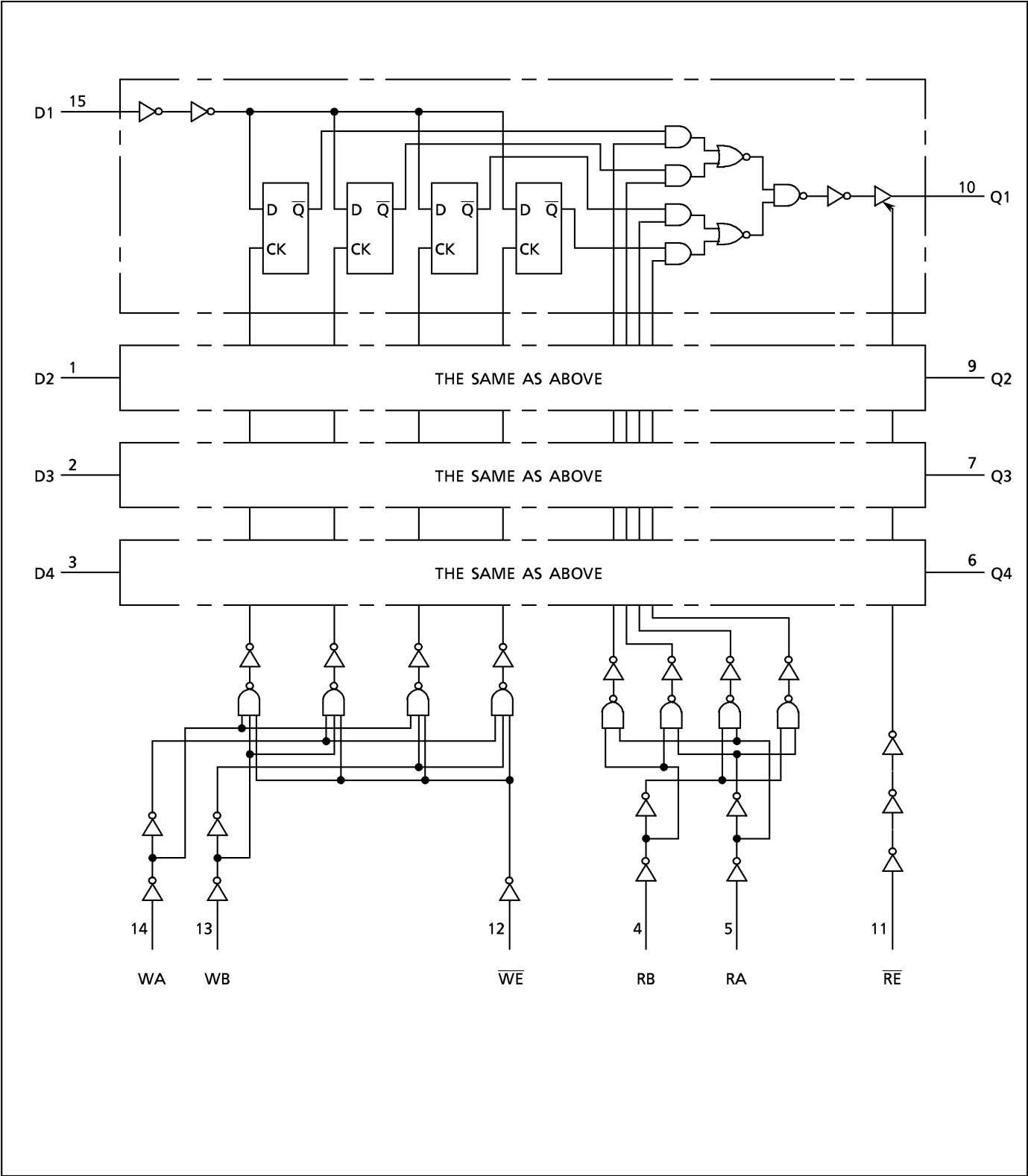
4. W0B1 : The first bit of word 0, etc.

Z : High Impedance

BLOCK DIAGRAM



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7.0$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} /Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	$^{\circ}\text{C}$

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ should be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	$^{\circ}\text{C}$
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$ ($V_{CC} = 2.0\text{V}$) $0 \sim 500$ ($V_{CC} = 4.5\text{V}$) $0 \sim 400$ ($V_{CC} = 6.0\text{V}$)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Input Voltage	V_{IL}		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20\mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	V
				4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20\mu\text{A}$	2.0 4.5 6.0	— — —	0.0 0.0 0.1	— — —	0.1 0.1 0.1	V
				4.5 6.0	— —	0.17 0.18	— —	0.33 0.33	
3 - State Output Off - State Current	I_{OZ}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = V_{CC} \text{ or GND}$	6.0	—	—	± 0.5	—	± 5.0	μA
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC} \text{ or GND}$	6.0	—	—	± 0.1	—	± 1.0	
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC} \text{ or GND}$	6.0	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		Ta = -40~85°C		UNIT
			V _{CC} (V)	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (WE)	$t_{W(L)}$		2.0 4.5 6.0	— — —	75 15 13	95 19 16	ns
Minimum Set-up Time (Dn—WE)	t_s		2.0 4.5 6.0	— — —	50 10 9	65 13 11	
Minimum Set-up Time (WA, WB—WE)	t_s		2.0 4.5 6.0	— — —	0 0 0	0 0 0	
Minimum Hold Time (Dn—WE)	t_h		2.0 4.5 6.0	— — —	5 5 5	5 5 5	
Minimum Hold Time (WA, WB—WE)	t_h		2.0 4.5 6.0	— — —	0 0 0	0 0 0	
Minimum Latch Time (WE—RA, RB)	t_{latch}	Note(1)	2.0 4.5 6.0	— — —	75 15 13	95 19 16	

Note(1): t_{latch} is the time allowed for the internal output of the latch to assume the state of new data.

This is important only when attempting to read from a location immediately after that location has received new data.

AC ELECTRICAL CHARACTERISTICS (C_L = 15pF, V_{CC} = 5V, Ta = 25°C, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		—	4	8	ns
Propagation Delay Time (RA, AB—Qn)	t_{pLH} t_{pHL}		—	23	34	
Propagation Delay Time (WE—Qn)	t_{pLH} t_{pHL}		—	24	38	
Propagation Delay Time (Dn—Qn)	t_{pLH} t_{pHL}		—	22	32	
3—State Output Enable Time	t_{pZL} t_{pZH}	R _L = 1kΩ	—	11	18	
3—State Output Disable Time	t_{pLZ} t_{pHZ}	R _L = 1kΩ	—	11	15	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}(\text{V})$	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation Delay Time (RA, AB—Qn)	t_{pLH} t_{pHL}		2.0	—	90	195	—	245	
			4.5	—	27	39	—	49	
			6.0	—	22	33	—	42	
Propagation Delay Time (WE—Qn)	t_{pLH} t_{pHL}		2.0	—	95	220	—	275	
			4.5	—	28	44	—	55	
			6.0	—	22	37	—	47	
Propagation Delay Time (Dn—Qn)	t_{pLH} t_{pHL}		2.0	—	90	185	—	230	
			4.5	—	26	37	—	46	
			6.0	—	20	31	—	39	
Output Enable time	t_{pZH} t_{pZL}	$R_L = 1\text{k}\Omega$	2.0	—	46	110	—	140	
			4.5	—	14	22	—	28	
			6.0	—	12	19	—	24	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L = 1\text{k}\Omega$	2.0	—	25	95	—	120	
			4.5	—	14	19	—	24	
			6.0	—	12	16	—	20	
Input Capacitance	C_{IN}			—	5	10	—	10	pF
Output Capacitance	C_{OUT}			—	10	—	—	—	
Power Dissipation Capacitance	$C_{PD} (1)$			—	101	—	—	—	

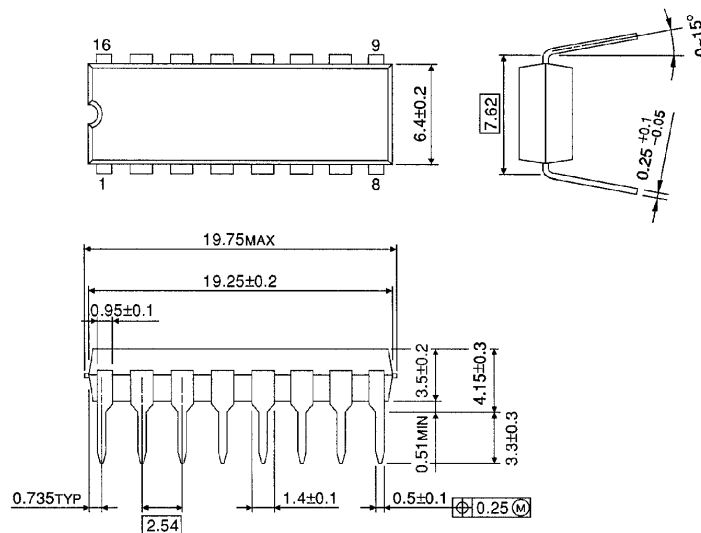
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

DIP 16PIN PACKAGE DIMENSIONS (DIP16-P-300-2.54)

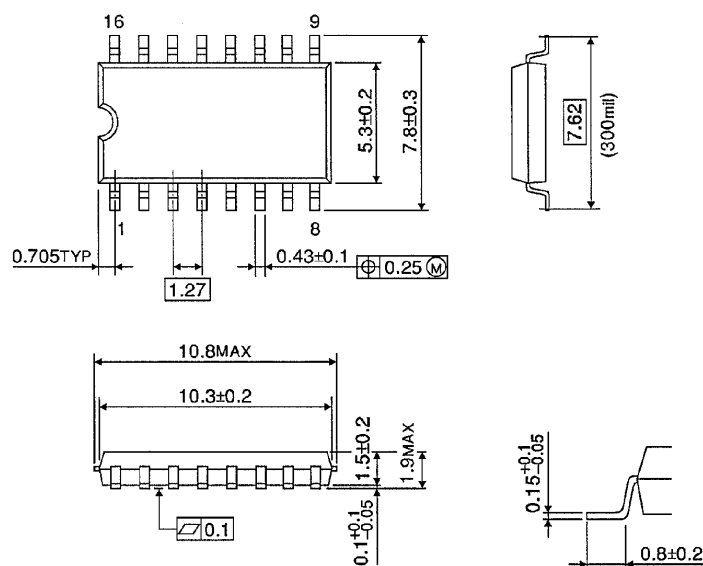
Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27)

Unit in mm



Weight : 0.18g (Typ.)

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