Design Example Report

Title	***Low Profile T8 (<10 mm), 23 W, Isolated, Power Factor Corrected (PF >0.9), LED Driver Using LinkSwitch™-PH LNK419EG***
Specification	185 VAC – 265 VAC Input; 50 V, 430 mA Output
Application	LED Driver for Low Profile T8
Author	Applications Engineering Department
Document Number	DER-318
Date	March 7, 2012
Revision	1.0

Summary and Features

- Low cost
  - Single-stage converter
  - Single sided PCB
  - Low component count
- Low profile (less than 10 mm component height)
- Highly energy efficient
  - ≥87% at 230 VAC
- Low THD, meets Class C harmonic limits
- Provides 1 kV differential surge protection
- IEC 61000-4-5 ring wave, IEC 61000-3-2 C harmonics and EN55015 B conducted EMI compliant
- Integrated protection and reliability features
  - Output open circuit / output short-circuit protected with auto-recovery
  - Line input overvoltage shutdown extends voltage withstand during line faults
  - Auto-recovering thermal shutdown with large hysteresis protects both components and printed circuit board

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Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

The document describes a low profile T8 (<10 mm component height), isolated, high power factor (PF) LED driver designed to drive a nominal LED string voltage of 50 V at 430 mA from an input voltage range of 185 VAC to 265 VAC. The LED driver utilizes the LNK419EG from the LinkSwitch-PH family of ICs.

Key Goals for this design were:

- Fit into narrow (<20 mm, component height <10 mm) T8 lamp enclosure
- Meet Class C harmonic limit to allow paralleling two LED drivers (>25 W) in a single fixture where Class C is then required
- Pass 1 kV differential surge

The topology is a single-stage, power factor corrected continuous conduction mode flyback that meets high efficiency, high power factor, low THD, isolation, low component count, and meets stringent space requirements.

High power factor and low THD is achieved by employing the LinkSwitch-PH IC which also provides a sophisticated range of protection features including auto-restart for open control loop and output short-circuit conditions.

This document contains the LED driver specification, schematic, PCB diagram, bill of materials, transformer documentation and typical performance characteristics.

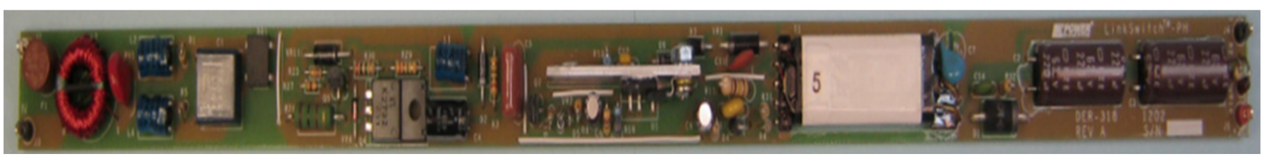

Figure 1 – Populated Circuit Board Photograph (Top View).

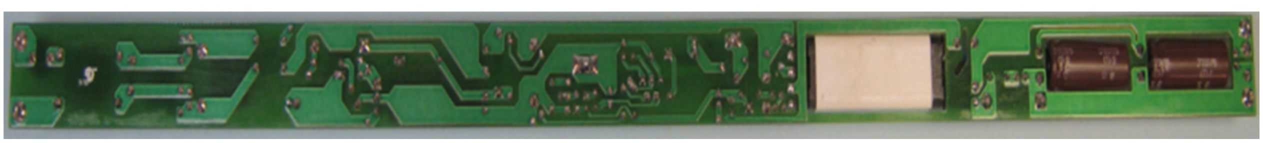

Figure 2 – Populated Circuit Board Photograph (Bottom View).

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	185	230	265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}		50		Hz	
Output						
Output Voltage	V_{OUT}	48	50	52	V	
Output Current	I_{OUT}		430		mA	V_{OUT} = 50, V_{IN} = 230 VAC, 25 °C
Total Output Power						
Continuous Output Power	P_{OUT}			23	W	
Efficiency						
Full Load	η	87			%	Measured at P_{OUT} 25 °C
Environmental						
Conducted EMI		CISPR 15B / EN55015B				
Safety		Isolated				
Surge (1.2 µ / 50 µ) Differential Mode (L1-L2)			1		kV	
Power Factor		0.9				Measured at $V_{OUT(TYP)}$, $I_{OUT(TYP)}$ and 230 VAC, 50 Hz
Harmonic Currents		EN 61000-3-2 Class C				
Ambient Temperature	T_{AMB}	40			°C	Free convection, sea level

3 Schematic

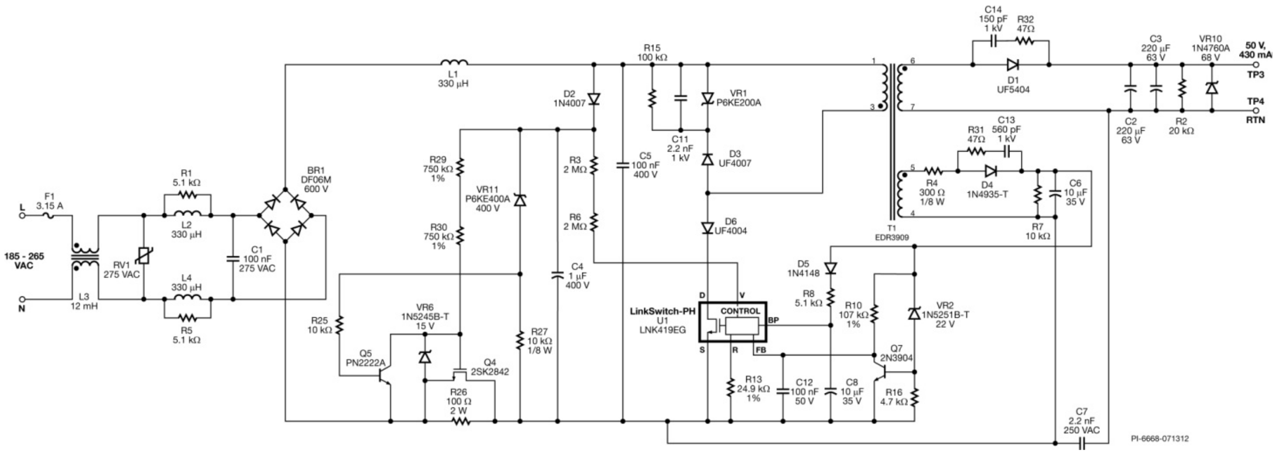

Figure 3 – Schematic.

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4 Circuit Description

The LinkSwitch-PH device is a controller with an integrated 725 V power MOSFET for use in LED driver applications. The LinkSwitch-PH is configured for use in a single-stage flyback topology which provides a primary side regulated constant current output while maintaining high power factor from the AC input.

4.1 Input Filtering

Fuse F1 provides protection from component failure and RV1 provides a clamp to limit the maximum voltage during differential line surge events. A 275 VAC rated part was selected, being slightly above the maximum specified operating voltage of 265 VAC. Diode bridge BR1 rectifies the AC line voltage with capacitor C5 providing a low impedance path (decoupling) for the primary switching current.

EMI filtering is provided by common mode inductor L3, and differential inductors L2 and L4 with an X capacitor C1. Resistor R1 and R5 across L2 and L4 damp any LC resonances due to the filter components and the AC line impedance, which would ordinarily show up on the conducted EMI measurements.

4.2 LinkSwitch-PH Primary

One side of the transformer (T1) is connected to the DC bus and the other to the DRAIN (D) pin of the LinkSwitch-PH thru the blocking diode D6. During the on-time of the power MOSFET, current ramps through the primary, storing energy which is then delivered to the output during the power MOSFET off-time. An EDR3909 core size was selected to meet both the power handling and size requirements of the design.

To provide peak line voltage information to U1 the incoming rectified AC peak charges C4 via D2. This is then fed into the VOLTAGE MONITOR (V) pin of U1 as a current via R3 and R6.

The V pin current and the FEEDBACK (FB) pin current are used internally to control the average output LED current. For non-dimming applications a 24.9 kΩ resistor is used on the REFERENCE (R) pin (R13) and 4 MΩ (R3 and R6) on the V pin. The value of 24.9 kΩ set both the UV threshold and line regulation suitable for non-TRIAC dimming applications.

During the power MOSFET off-time, D3, R15, C11 and VR1 clamp the drain voltage to a safe level due to the effects of leakage inductance.

Diode D4, C6, and R7 generate a primary bias supply from an auxiliary winding on the transformer. C7 is used to minimize the loop on the bias winding circuit for reduced EMI. Resistors R4, R31, and C13 provide filtering so that the bias voltage tracks the output voltage closely (to maintain constant output current with changes in LED voltage).

Capacitor C8 provides local decoupling for the BYPASS (BP) pin of U1 which is the supply pin for the internal controller. During start-up, C8 is charged to ~6 V from an internal high-voltage current source connected to the D pin. Once charged U1 starts switching at which point the operating supply current is provided from the bias supply via R8. Capacitor C8 also selects the output power mode, 10 μF was selected (reduced power mode) to minimize the device dissipation and minimize heat sinking requirements.

4.3 Feedback

The bias winding voltage is used to sense the output voltage indirectly, eliminating secondary-side feedback components. The voltage on the bias winding is proportional to the output voltage (set by the turn ratio between the bias and secondary windings). Resistor R10 converts the bias voltage into a current which is fed into the FB pin of U1. The internal engine within U1 combines the FB pin current, the V pin current, and internal drain current information to provide a constant output current while maintaining high input power factor.

4.4 Output Rectification

The transformer secondary winding is rectified by D1 and filtered by C2 and C3. For designs where higher ripple is acceptable, the output capacitance value can be reduced (and for lower ripple increased). In the case of an open load condition, Zener diode VR10 will limits the output voltage. The unit enters auto-restart operation when Q7 turns on, with Zener diode VR2 setting the overvoltage limit.

4.5 High Surge Protection Circuit

High-voltage differential AC line surges will cause the bus voltage to exceed the voltage rating of U1 due to the limited capacitance (C4 + C5) after the bridge. To further limit the voltage R26 is connected in series with the output of the bridge rectifier. A significant proportion of the voltage now appears across the series resistor during the surge, reducing the voltage across C5 and U1.

To prevent excessive power dissipation in the resistor, it is shorted by Q4 during normal operation. Zener diode VR11 sets the threshold of 400 V. Above this level, Q5 turns on, pulling the gate of Q4 low and connecting R26 in circuit. Below this level the gate of Q4 is clamped to 15 V by VR6.

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5 PCB Layout

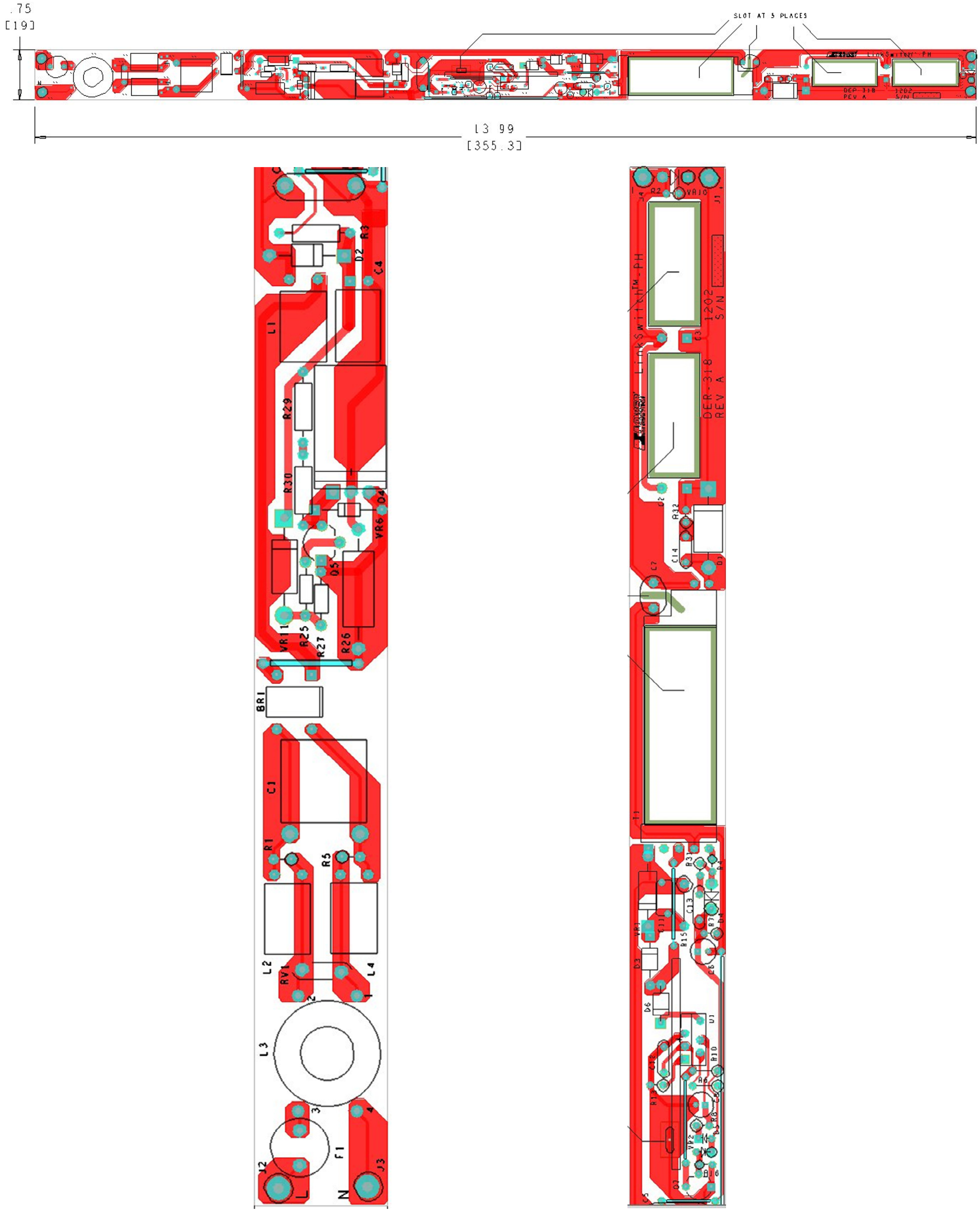

Figure 4 – PCB Layout, Outline and Silkscreen.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	600 V, 1 A, Bridge Rectifier, DFM package	DF06M	Diodes, Inc.
2	1	C1	100 nF, 275 VAC, Film, X2	LE104-M	OKAYA
3	2	C2 C3	220 μF, 63 V, Electrolytic, Gen. Purpose, (10 x 25)	EKZE630ELL221MJ25S	United Chemi-con
4	1	C4	1 μF, 400 V, Electrolytic, (6.3 x 11)	EKMG401ELL1R0MF11D	United Chemi-Con
5	1	C5	100 nF, 400 V, Film	ECQ-E4104KF	Panasonic
6	2	C6 C8	10 μF, 35 V, Electrolytic, Gen Purpose, (5 x 11)	UPW1V100MDD6	Nichicon
7	1	C7	2.2 nF, 250 VAC, Film, X1Y1	DE2E3KY222MA2BM01	Murata
8	1	C11	2200 pF, 1 kV, Disc Ceramic	562R5GAD22	Vishay
9	1	C12	100 nF, 50 V, Ceramic, Z5U, .2 Lead Space	C317C104M5U5TA	Kemet
10	1	C13	560 pF, 1 kV, Disc Ceramic	ECK-A3A561KBP	Panasonic
11	1	C14	150 pF, 1 kV, Disc Ceramic	NCD151K1KVY5F	NIC
12	1	D1	400 V, 3 A, Ultrafast Recovery, 75 ns, DO-201AD	UF5404-E3	Vishay
13	1	D2	1000 V, 1 A, Rectifier, DO-41	1N4007-E3/54	Vishay
14	1	D3	1000 V, 1 A, Ultrafast Recovery, 75 ns, DO-41	UF4007-E3	Vishay
15	1	D4	200 V, 1 A, Fast Recovery, 200 ns, DO-41	1N4935-T	Diodes, Inc.
16	1	D5	75 V, 300 mA, Fast Switching, DO-35	1N4148TR	Vishay
17	1	D6	400 V, 1 A, Ultrafast Recovery, 50 ns, DO-41	UF4004-E3	Vishay
18	1	F1	3.15 A, 250 V, Slow, TR5	37213150411	Wickman
19	1	J1	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
20	1	J2	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
21	2	J3 J4	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
22	3	L1 L2 L4	330 μH, 0.34 A, 7 x 10.5 mm	SBC2-331-341	Tokin
23	1	L3	12 mH, 200 mA, Common Mode Choke		
24	1	Q4	600 V, 4 A, 1200 mΩ, N-Channel, TO-220F	2SK2792	Rohm Semi
25	1	Q5	NPN, Small Signal BJT, 40 V, 0.6 A, TO-92	PN2222AG	On Semi
26	1	Q7	NPN, Small Signal BJT, 40 V, 0.2 A, TO-92	2N3904RLRAG	On Semi
27	2	R1 R5	5.1 kΩ, 5%, 1/8 W, Carbon Film	CFR-12JB-5K1	Yageo
28	1	R2	20 kΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-20K	Yageo
29	4	R3 R6 R29 R30	2.0 MΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-2M0	Yageo
30	1	R4	300 Ω, 5%, 1/8 W, Carbon Film	CFR-12JB-300R	Yageo
31	1	R7	10 kΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-10K	Yageo
32	1	R8	5.1 kΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-5K1	Yageo
33	1	R10	107 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-107K	Yageo
34	1	R13	24.9 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-24K9	Yageo
35	1	R15	100 kΩ, 5%, 1/2 W, Carbon Film	CFR-50JB-100K	Yageo
36	1	R16	4.7 kΩ, 5%, 1/8 W, Carbon Film	CFR-12JB-4K7	Yageo
37	2	R25 R27	10 kΩ, 5%, 1/8 W, Carbon Film	CFR-12JB-10K	Yageo

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38	1	R26	100 Ω, 5%, 2 W, Metal Oxide	RSMF2JT100R	Stackpole
39	2	R31 R32	47 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-47R	Yageo
40	1	RV1	275 V, 23 J, 7 mm, RADIAL	V275LA4P	Littlefuse
41	1	T1	Bobbin, EDR-3909, Horizontal, 8 pins		SBEF
42	1	TE1	Terminal, Eyelet, Tin Plated Brass, Zierick PN 190	190	Zierick
43	1	U1	LinkSwitch-PH, eSIP	LNK419EG	Power Integrations
44	1	VR1	200 V, 5 W, 5%, TVS, DO204AC (DO-15)	P6KE200ARLG	On Semi
45	1	VR2	22 V, 5%, 500 mW, DO-35	1N5251B-T	Diodes, Inc.
46	1	VR6	15 V, 5%, 500 mW, DO-35	1N5245B-T	Diodes, Inc.
47	1	VR10	68 V, 5%, 1 W, DO-41	1N4760A	Micro Semi
48	1	VR11	400 V, 600 W, 5%, TVS, DO204AC (DO-15)	P6KE400A	Littlefuse

7 Heat Sink Assembly

7.1 Heat Sink Fabrication Drawing

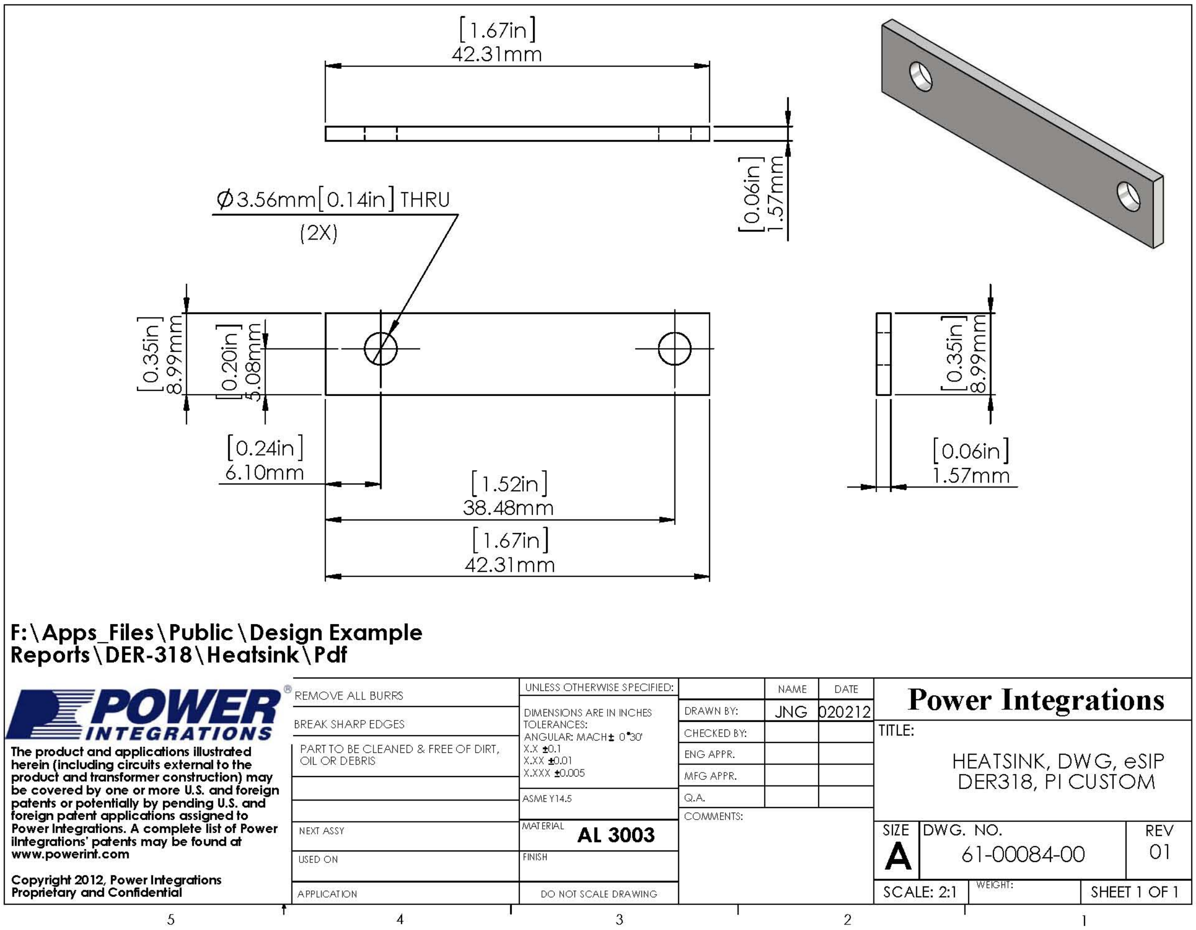

Figure 5 – Heat Sink Fabrication Drawing.

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7.2 Heat Sink Assembly Drawing

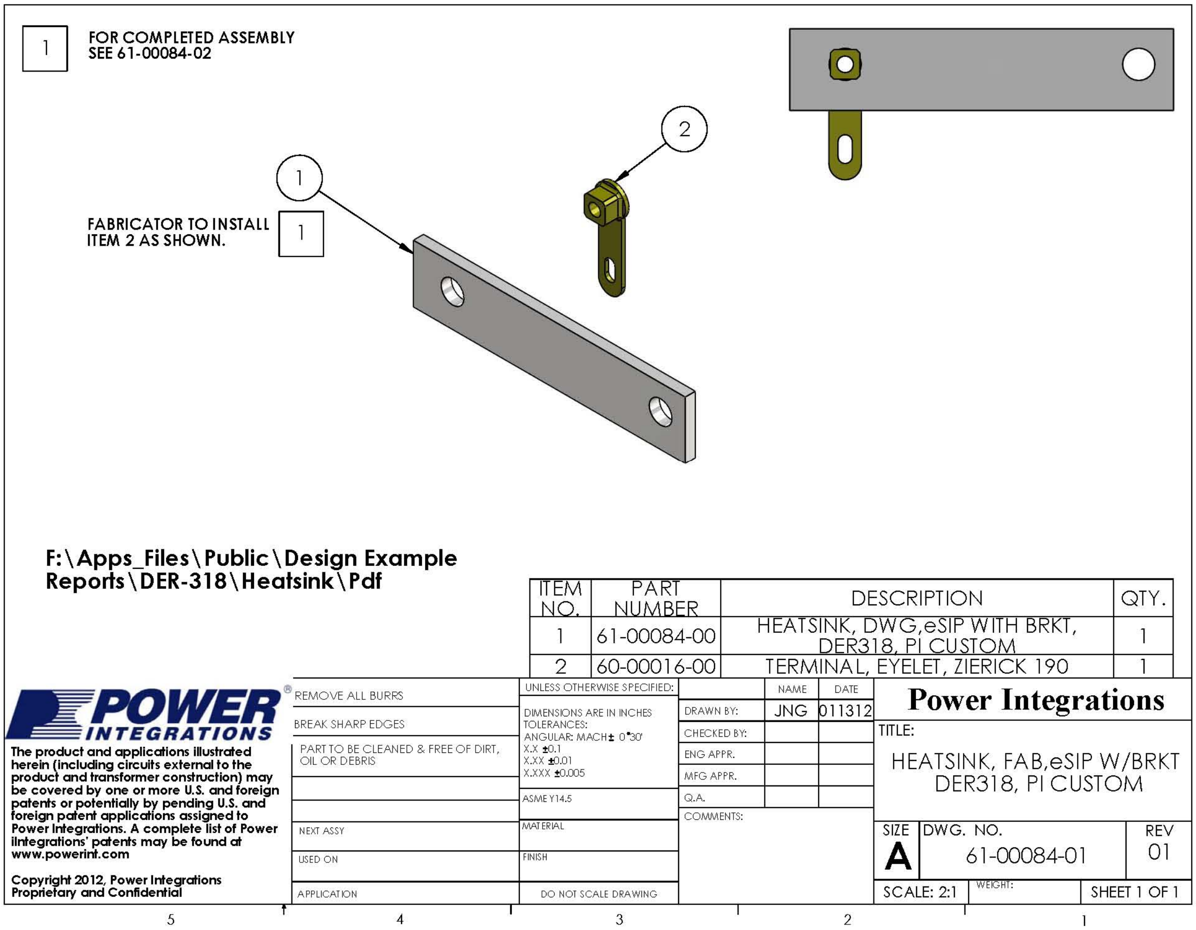
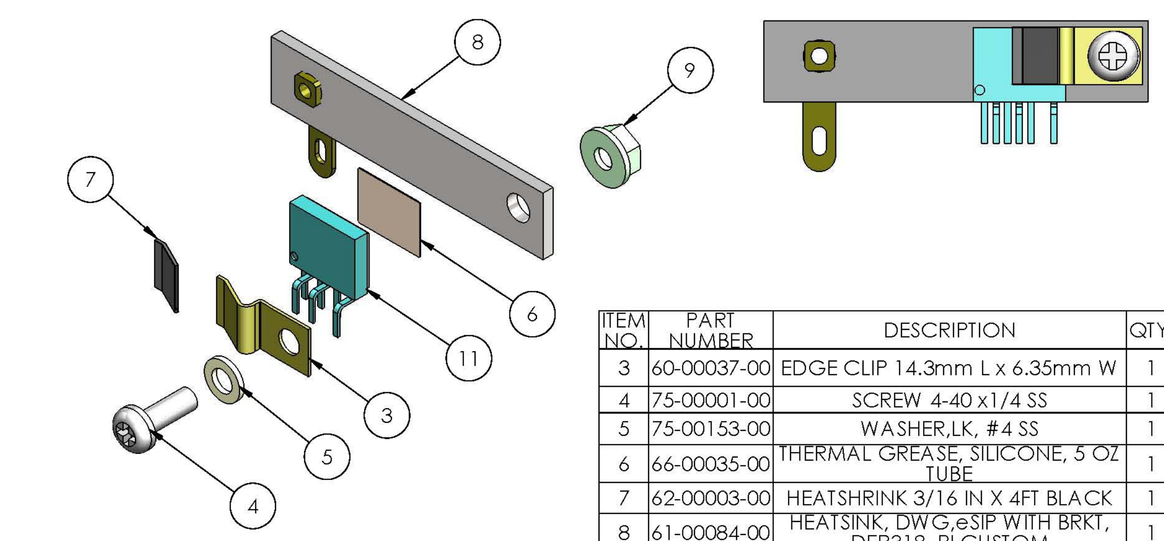


Figure 6 – Heat Sink Assembly Drawing.

7.3 Heat Sink and LinkSwitch-PH Assembly Drawing



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
3	60-00037-00	EDGE CLIP 14.3mm L x 6.35mm W	1
4	75-00001-00	SCREW 4-40 x1/4 SS	1
5	75-00153-00	WASHER,LK, #4 SS	1
6	66-00035-00	THERMAL GREASE, SILICONE, 5 OZ TUBE	1
7	62-00003-00	HEATSHRINK 3/16 IN X 4FT BLACK	1
8	61-00084-00	HEATSINK, DWG,eSIP WITH BRKT, DER318, PI CUSTOM	1
9	75-00068-00	NUT,HEX,KEP4-40, ZINC PLATE	1
10	60-00016-00	TERMINAL, EYELET, ZIERICK 190	1
11	10-00483-00	LINKSWITCH, LNK419EG,eSIP	1

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REMOVE ALL BURRS
BREAK SHARP EDGES
PART TO BE CLEANED & FREE OF DIRT, OIL OR DEBRIS
NEXT ASSY
USED ON
APPLICATION

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES:
ANGULAR: MACH± 0°30'
X.X ±0.1
X.XX ±0.01
X.XXX ±0.005
ASME Y14.5
MATERIAL
FINISH
DO NOT SCALE DRAWING

	NAME	DATE
DRAWN BY:	JNG	011312
CHECKED BY:		
ENG APPR.		
MFG APPR.		
Q.A.		

COMMENTS:

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TITLE:
HEATSINK, ASSY,eSIP W/BRKT, DER18, PI CUSTOM

SIZE A | DWG. NO. 61-00084-02 | REV 01

SCALE: 1:1 | WEIGHT: | SHEET 1 OF 1

5 4 3 2 1

Figure 7 – Heat Sink and LinkSwitch-PH Assembly Drawing.

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8 Common Mode Inductor Specification

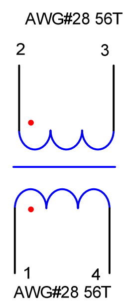


Figure 8 – CMC Electrical Diagram.

8.1 *Electrical Specifications*

Inductance (LCM)	Pins 1-4 or 2-3 measured at 100 kHz	12 mH ±10%
Leakage (LL)	Pins 1-4 with pins 2-3 shorted or versa at 100 kHz	80 µH (Max.) ±20%
Core Effective Inductance		3795 nH/N²

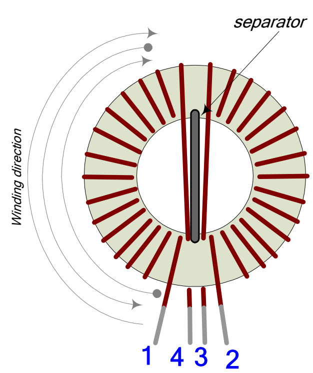
8.2 *Materials*

Item	Description
[1]	Toroid Core: MN-ZN T1 4x 9 x 5 R10K U1000; Dimension: OD:14.35 mm / ID:7.5 mm / HT:5.3 mm
[2]	Magnet Wire: #28 AWG, Heavy Nyleze

8.3 *Winding Instructions*

- Use 4 ft of item [2], start at pin 1 wind 56 turns end at pin 4.
- Do the same for another half of Toroid, start at pin 2 and end at pin 3.

8.4 *Illustrations*



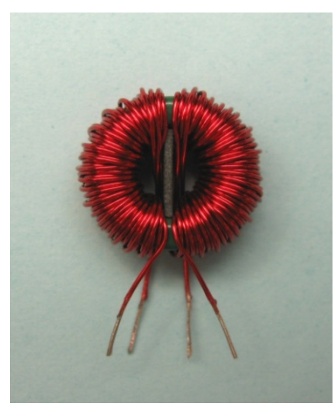


Figure 9 – CMC Build Illustration.

9 Transformer Specification

9.1 Electrical Diagram

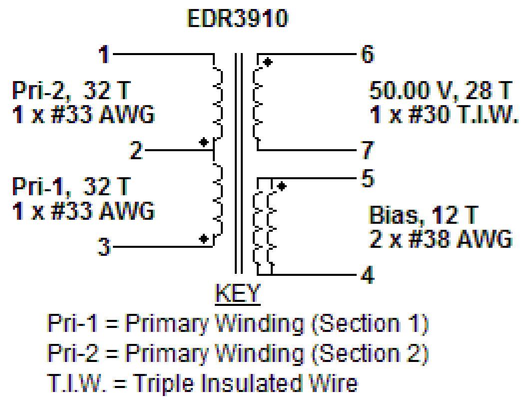


Figure 10 – Transformer Electrical Diagram.

9.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1-3 to pins 6-7	3000 VAC
Primary Inductance	Pins 1-3, all other windings open, measured at 100 kHz, 0.4 V_{RMS}	2700 μH, ±7%
Resonant Frequency	Pins 1-3, all other windings open	500 kHz (Min.)
Primary Leakage Inductance	Pins 1-3, with pins 6-7 shorted, measured at 100 kHz, 0.4 V_{RMS}	50 μH (Max.)

9.3 Materials

Item	Description
[1]	Core: EDR3909, AL= 659 nH/N^2
[2]	Bobbin: Vertical Generic, 5 pri. + 2 sec.
[3]	Barrier Tape: Polyester film [1 mil (25 um) base thickness], 3.70 mm wide
[4]	Varish
[5]	Magnet Wire: #33 AWG
[6]	Magnet Wire: #30 AWG Triple-insulated Wire
[7]	Magnet Wire: #38 AWG
[8]	Copper tape: 3.5 mm

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9.4 Transformer Build Diagram

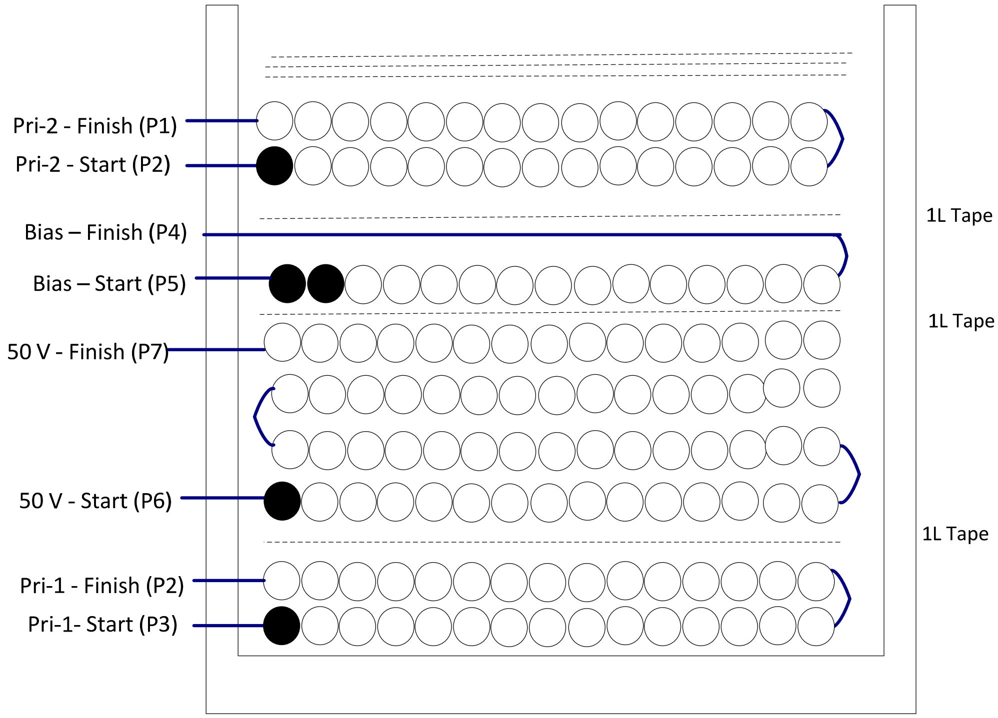

Figure 11 – Transformer Build Diagram.

9.5 Transformer Construction

Bobbin Preparation	Pull-out pin number 8. Position the bobbin such that the pins are on the left side of the bobbin chuck. Machine rotates in forward direction.
WDG1 Primary 1	Start at pin 3; wind with firm tension 32 turns of item [5] from left to right. Finish at pin 2.
Insulation	1 layer of tape [3] for insulation.
WDG2 Secondary	Start at pin 6; wind with firm tension 28 turns of item [6] in continuously in four layers from left to right. Finish at pin 7.
Insulation	1 layer of tape [3] for insulation.
WDG3 Bias	Start at pin 5; wind with firm tension 12 bifilar turns item [7]. Finish at pin 4.
Insulation	1 layer of tape [3] for insulation.
WDG4 Primary 2	Start at pin 2; wind with firm tension 32 turns of item [5] from left to right. Finish at pin 1.
Insulation	3 layers of tape [3] for insulation.
Assemble Core	Assemble and secure the cores.
Copper Shield	Add 1 turn of copper shield around the core.
Finish	Varnish transformer assembly.

10 Transformer Design Spreadsheet

ACDC_LinkSwitch-PH_102611; Rev.1.7; Copyright Power Integrations 2011	INPUT	INFO	OUTPUT	UNIT	LinkSwitch-PH_102611: Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
Dimming required	**NO**		**NO**		Select 'YES' option if dimming is required. Otherwise select 'NO'.
VACMIN	185		185	V	Minimum AC Input Voltage
VACMAX			265	V	Maximum AC input voltage
fL			50	Hz	AC Mains Frequency
VO	50		50	V	Typical output voltage of LED string at full load
VO_MAX			55	V	Maximum expected LED string Voltage.
VO_MIN			45	V	Minimum expected LED string Voltage.
V_OVP			60.5	V	Over-voltage protection setpoint
IO	0.43		0.43	A	Typical full load LED current
PO			21.5	W	Output Power
n	0.88		0.88		
VB			20	V	Bias Voltage
ENTER LinkSwitch-PH VARIABLES					
LinkSwitch-PH	**LNK419**		**LNK419**	Universal	115 Doubled/230V
Chosen Device		LNK419	Power Out	18W	8W
Current Limit Mode	**RED**		**RED**		Select "RED" for reduced Current Limit mode or "FULL" for Full current limit mode
ILIMITMIN			2.35	A	Minimum current limit
ILIMITMAX			2.73	A	Maximum current limit
fS			66000	Hz	Switching Frequency
fSmin			62000	Hz	Minimum Switching Frequency
fSmax			70000	Hz	Maximum Switching Frequency
IV			80.3	uA	V pin current
RV			3.909	M-ohms	Upper V pin resistor
RV2			1.402	M-ohms	Lower V pin resistor
IFB	114.71		114.7	uA	FB pin current (85 uA < IFB < 210 uA)
RFB1			148.2	k-ohms	FB pin resistor
VDS			10	V	LinkSwitch-PH on-state Drain to Source Voltage
VD	0.5		0.5	V	Output Winding Diode Forward Voltage Drop (0.5 V for Schottky and 0.8 V for PN diode)
VDB	0.7		0.7	V	Bias Winding Diode Forward Voltage Drop
Key Design Parameters					
KP	0.69		0.69		Ripple to Peak Current Ratio (For PF > 0.9, 0.4 < KP < 0.9)
LP			2693	uH	Primary Inductance
VOR	115.43		115.43	V	Reflected Output Voltage.
Expected IO (average)		Info	0.31	A	Expected Average Output current is outside 5% tolerance band. Change IFB to 157 for better current regulation set-point
KP_VACMAX			0.75		Expected ripple current ratio at VACMAX
TON_MIN			3.57	us	Minimum on time at maximum AC input voltage
PCLAMP			0.16	W	Estimated dissipation in primary clamp
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**EDR3910**		**EDR3910**		
Bobbin		#N/A		P/N:	#N/A
AE	1.04		1.04	cm^2	Core Effective Cross Sectional Area
LE	2		2	cm	Core Effective Path Length

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AL	5000		5000	nH/T^2	Ungapped Core Effective Inductance
BW	3.7		3.7	mm	Bobbin Physical Winding Width
M			0	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	4		4		Number of Primary Layers
NS	28		28		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			262	V	Peak input voltage at VACMIN
VMAX			375	V	Peak input voltage at VACMAX
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.31		Minimum duty cycle at peak of VACMIN
IAVG			0.12	A	Average Primary Current
IP			0.72	A	Peak Primary Current (calculated at minimum input voltage VACMIN)
IRMS			0.22	A	Primary RMS Current (calculated at minimum input voltage VACMIN)
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			2693	uH	Primary Inductance
NP			64		Primary Winding Number of Turns
NB			11		Bias Winding Number of Turns
ALG			657	nH/T^2	Gapped Core Effective Inductance
BM			2915	Gauss	Maximum Flux Density at PO, VMIN (BM<3100)
BP			3527	Gauss	Peak Flux Density (BP<3700)
BAC			1006	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			765		Relative Permeability of Ungapped Core
LG			0.17	mm	Gap Length (Lg > 0.1 mm)
BWE			14.8	mm	Effective Bobbin Width
OD			0.23	mm	Maximum Primary Wire Diameter including insulation
INS			0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.19	mm	Bare conductor diameter
AWG			33	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			51	Cmils	Bare conductor effective area in circular mils
CMA			234	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 600)
LP_TOL			10		Tolerance of primary inductance
TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE OUTPUT EQUIVALENT)					
Lumped parameters					
ISP			1.65	A	Peak Secondary Current
ISRMS			0.67	A	Secondary RMS Current
IRIPPLE			0.52	A	Output Capacitor RMS Ripple Current
CMS			135	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			28	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.32	mm	Secondary Minimum Bare Conductor Diameter
ODS			0.13	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
VOLTAGE STRESS PARAMETERS					
VDRAIN			610	V	Estimated Maximum Drain Voltage assuming maximum LED string voltage (Includes Effect of Leakage Inductance)
PIVS			224	V	Output Rectifier Maximum Peak Inverse Voltage (calculated at VOVP, excludes leakage inductance spike)
PIVB			91	V	Bias Rectifier Maximum Peak Inverse Voltage

					(calculated at VOVP, excludes leakage inductance spike)
FINE TUNING (Enter measured values from prototype)					
V pin Resistor Fine Tuning					
RV1	4		4	M-ohms	Upper V Pin Resistor Value
RV2	40		40	M-ohms	Lower V Pin Resistor Value
VAC1			115	V	Test Input Voltage Condition1
VAC2			230	V	Test Input Voltage Condition2
IO_VAC1	0.4		0.4	A	Measured Output Current at VAC1
IO_VAC2	0.43		0.43	A	Measured Output Current at VAC2
RV1 (new)			3.77	M-ohms	New RV1
RV2 (new)			0.6	M-ohms	New RV2
V_OV			314.6	V	Typical AC input voltage at which OV shutdown will be triggered
V_UV			76	V	Typical AC input voltage beyond which power supply can startup
FB pin resistor Fine Tuning					
RFB1			148	k-ohms	Upper FB Pin Resistor Value
RFB2			1.00E+12	k-ohms	Lower FB Pin Resistor Value
VB1			18	V	Test Bias Voltage Condition1
VB2			22	V	Test Bias Voltage Condition2
IO1			0.43	A	Measured Output Current at Vb1
IO2			0.43	A	Measured Output Current at Vb2
RFB1 (new)			148.2	k-ohms	New RFB1
RFB2(new)			1.00E+12	k-ohms	New RFB2
Input Current Harmonic Analysis					
Harmonic			Max Current (mA)	Limit (mA)	
1st Harmonic					
3rd Harmonic			19.32	1785.97	PASS. 3rd Harmonic current content is lower than the limit
5th Harmonic			8	998.04	PASS. 5th Harmonic current content is lower than the limit
7th Harmonic			4.6	525.28	PASS. 7th Harmonic current content is lower than the limit
9th Harmonic			3.14	262.64	PASS. 9th Harmonic current content is lower than the limit
11th Harmonic			2.36	183.85	PASS. 11th Harmonic current content is lower than the limit
13th Harmonic			1.81	155.54	PASS. 13th Harmonic current content is lower than the limit
15th Harmonic			1.37	134.79	PASS. 15th Harmonic current content is lower than the limit
THD			20.9	%	Estimated total Harmonic Distortion (THD)

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11 Performance Data

All measurements performed at room temperature using an LED load. The following data were measured using 3 sets of loads to represent a voltage of 48 V ~ 52 V. The table in Section 11.6 shows complete test data values.

11.1 Efficiency

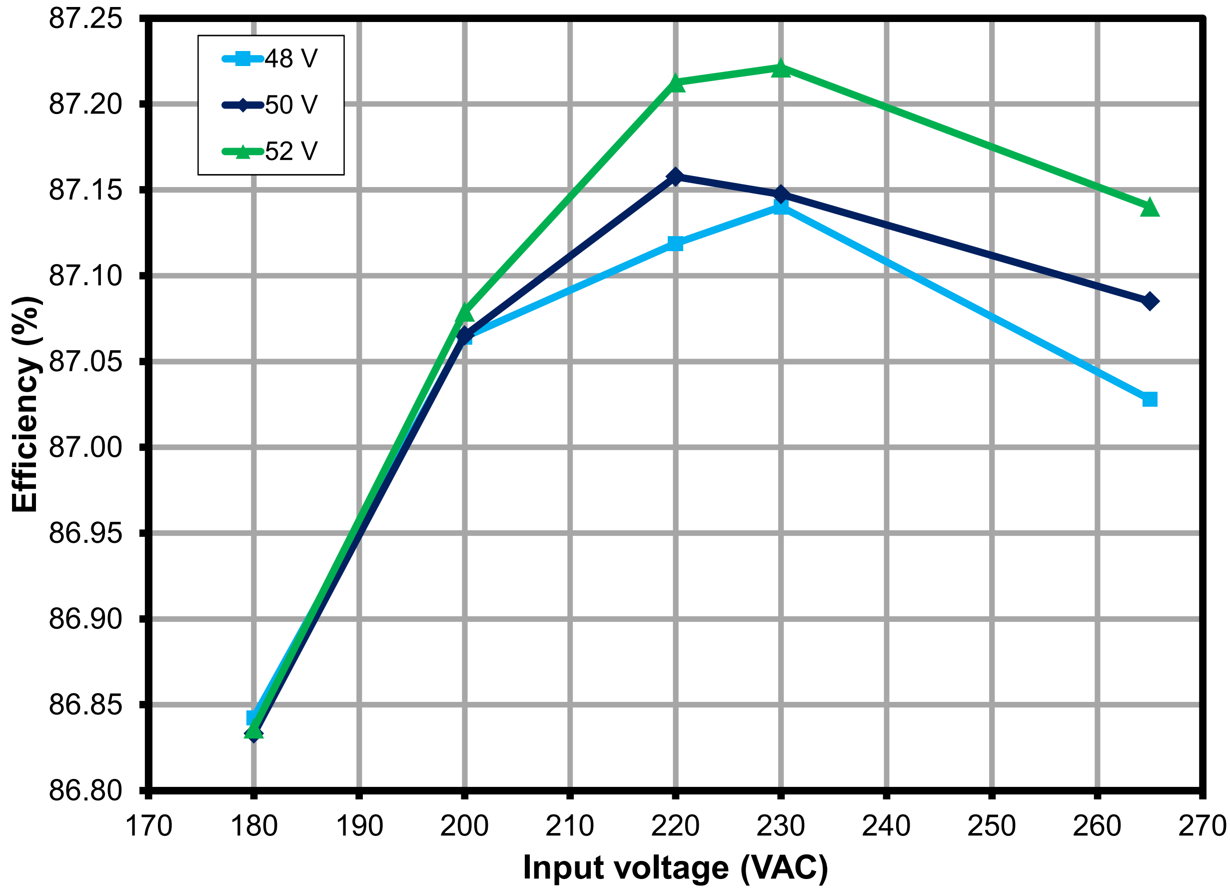

Figure 10 – Efficiency vs. Line and Load.

11.2 Line and Load Regulation

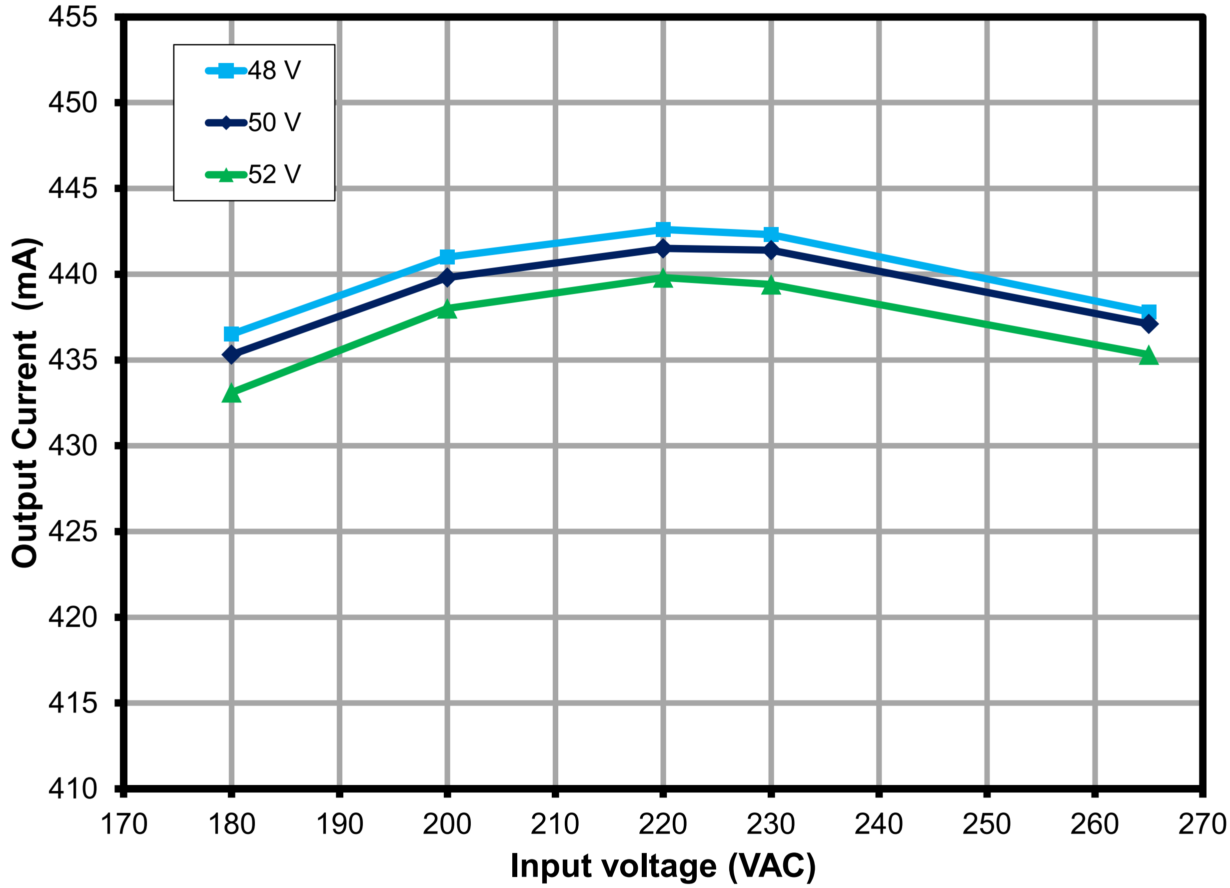

Figure 11 – Regulation vs. Line and Load.

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11.3 Power Factor

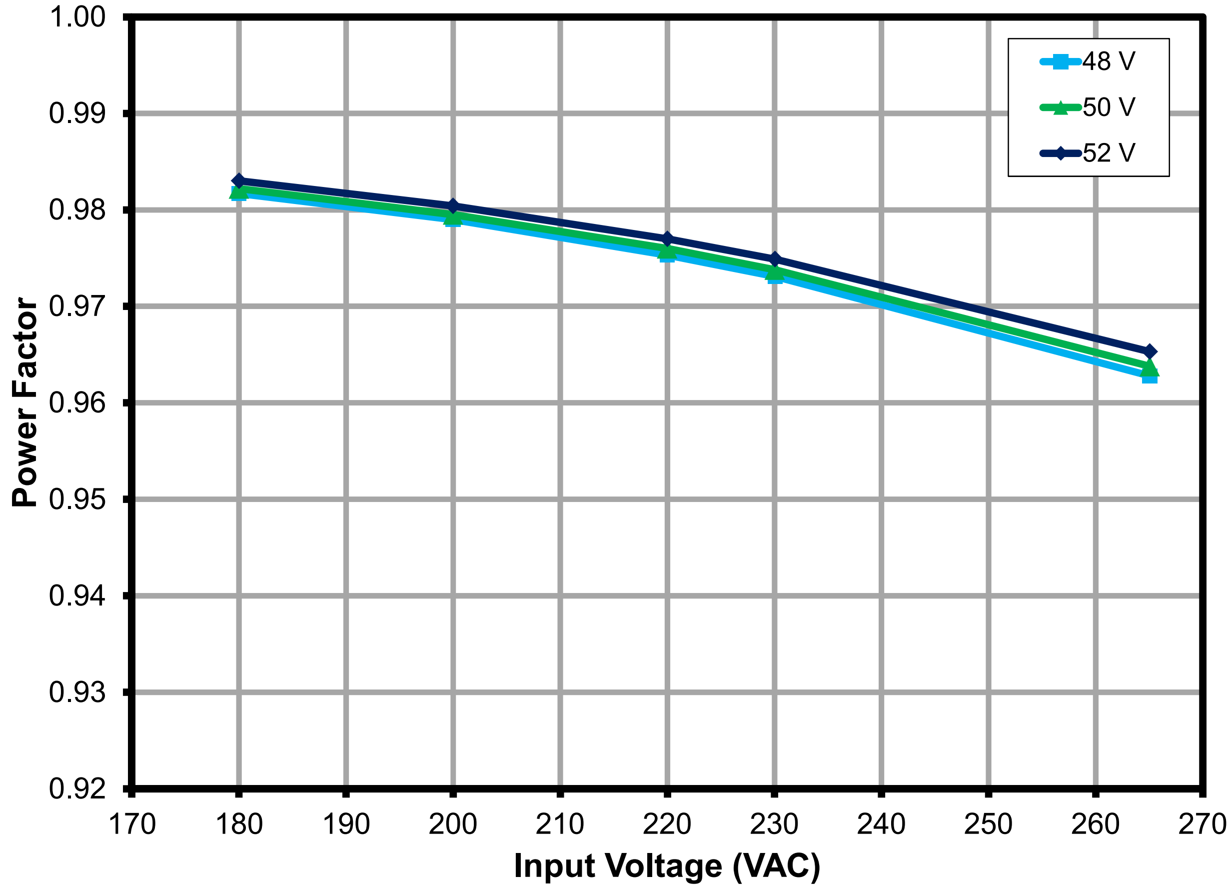

Figure 12 – Power Factor vs. Line and Load.

11.4 A-THD

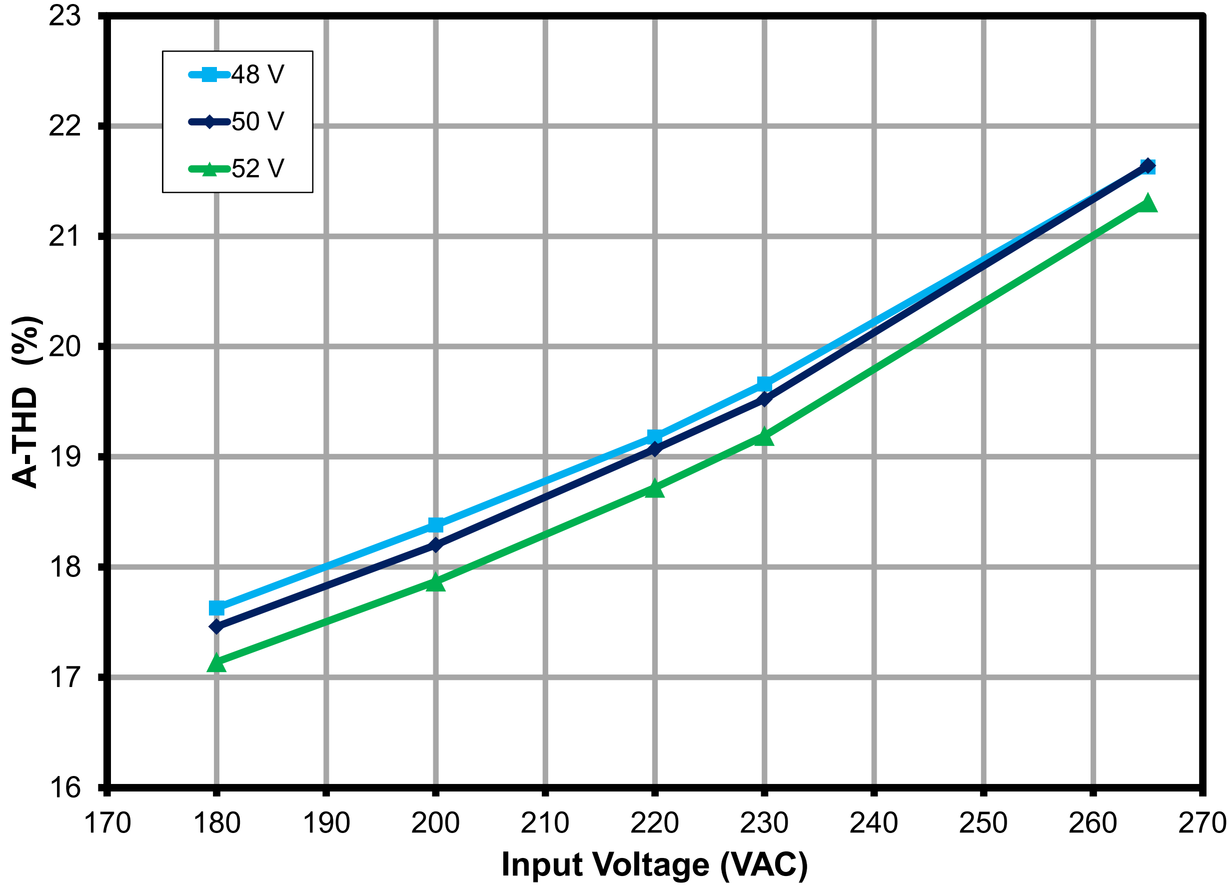

Figure 13 – A-THD vs. Line and Load.

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11.5 Harmonic Currents

The design met the limits for Class C equipment for an active input power of >25 W. Even in this case IEC61000-3-2 specifies that harmonic currents shall not exceed the limits of Class D equipment[1], the unit passed the Class C limit in case of paralleling multiple units.

11.5.1 48 V LED Load

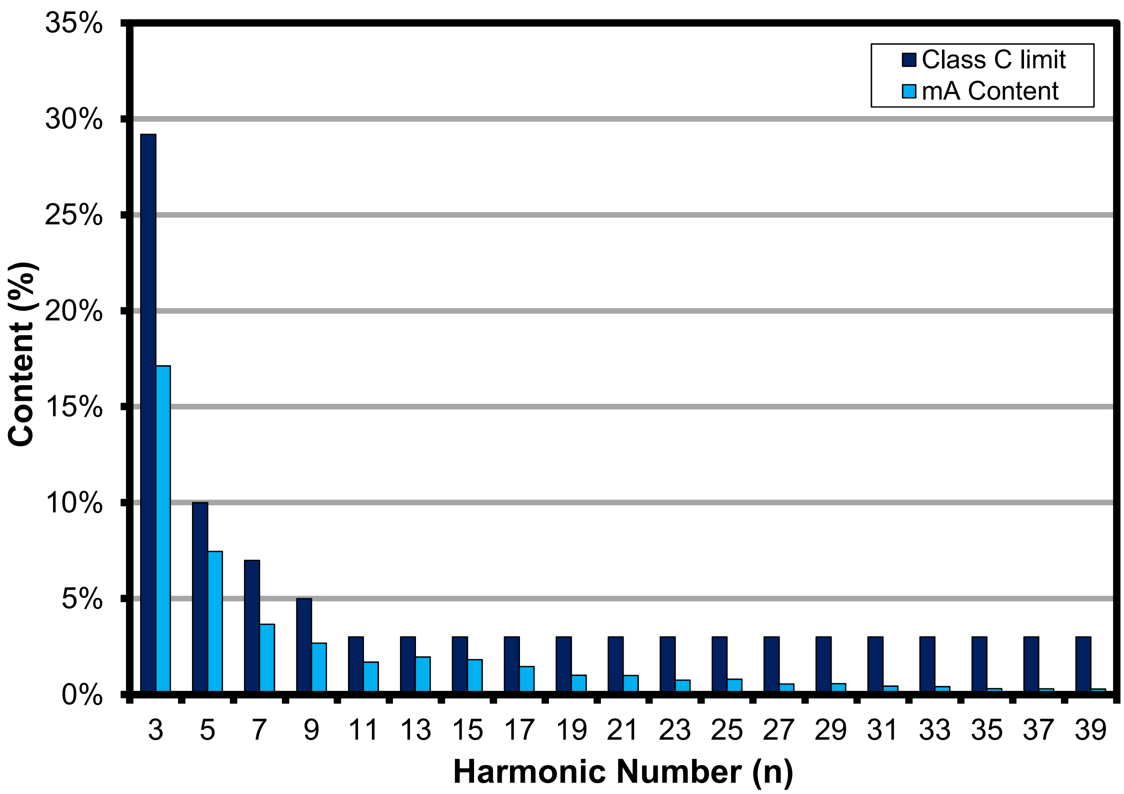

Figure 12 – 48 V LED Load Input Current Harmonics at 230 VAC, 50 Hz.

[1] IEC6000-3-2 Section 7.3, table 2, column 2.

11.5.2 50 V LED Load

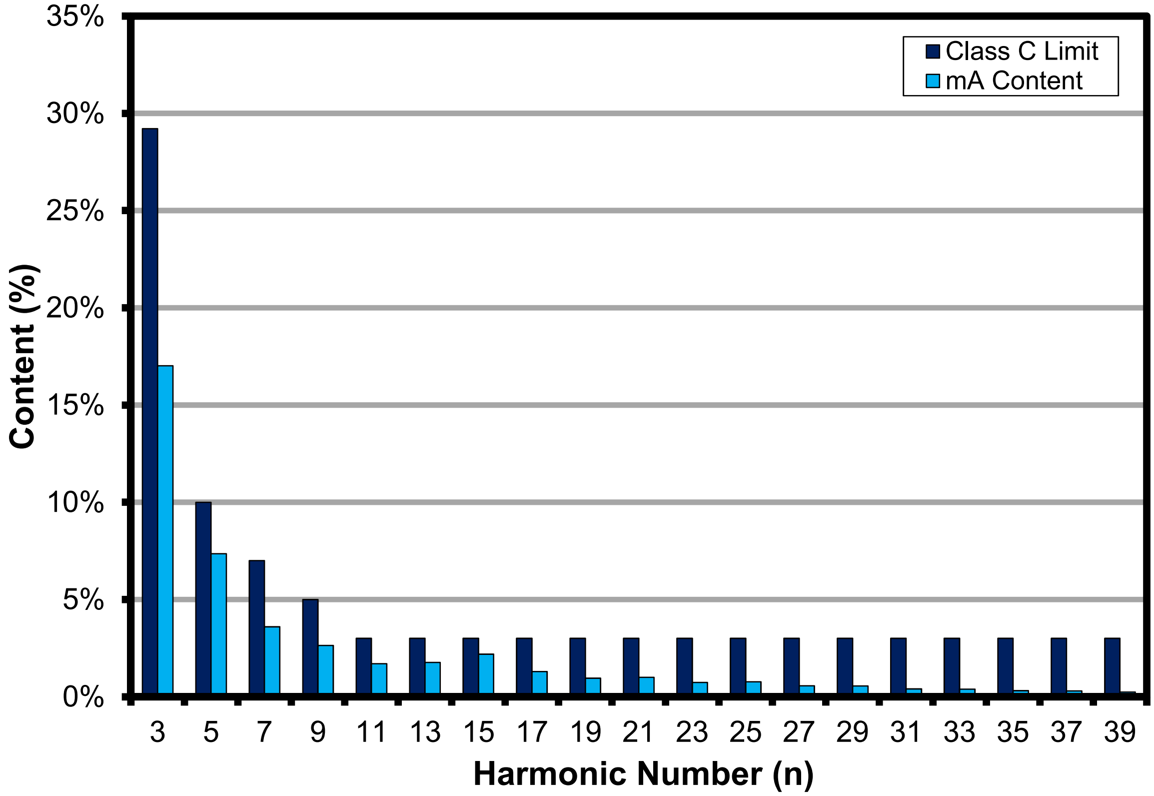

Figure 13 – 50 V LED Load Input Current Harmonics at 230 VAC, 50 Hz.

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11.5.3 52 V LED Load

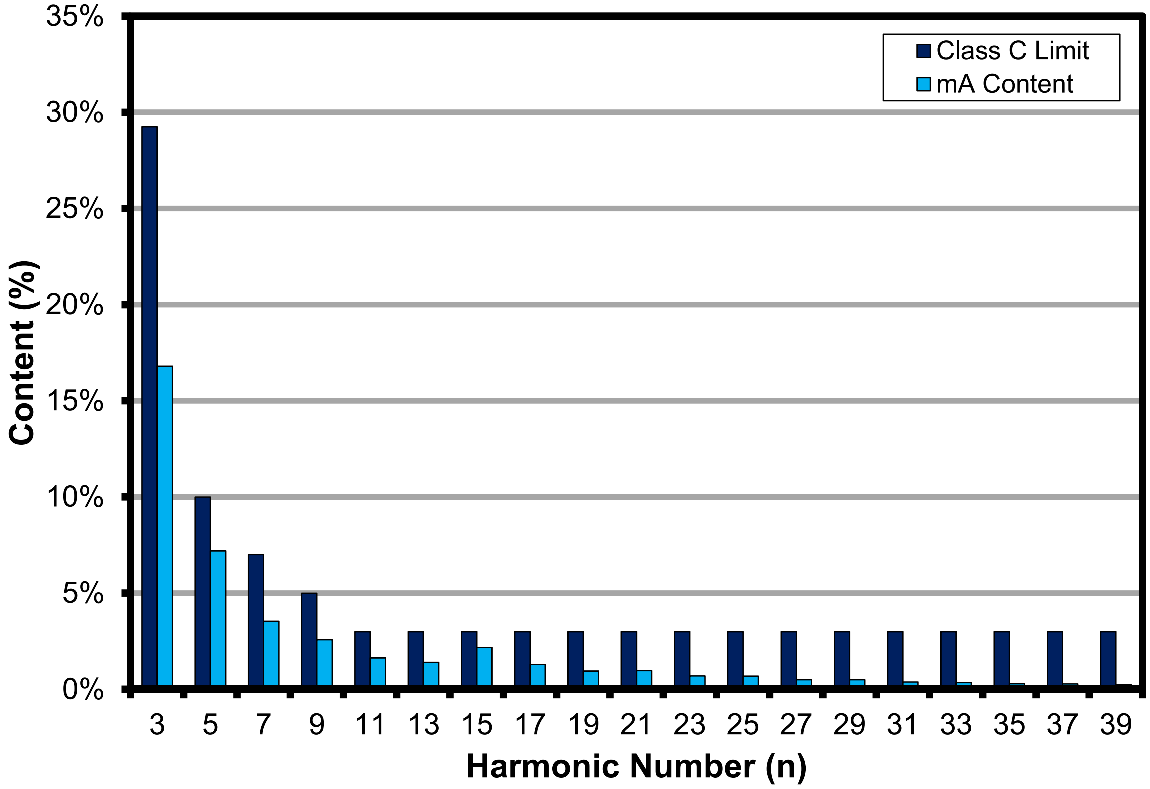

Figure 14 – 52 V LED Load Input Current Harmonics at 230 VAC, 50 Hz.

11.5.4 Two Drivers in Parallel (46 W)

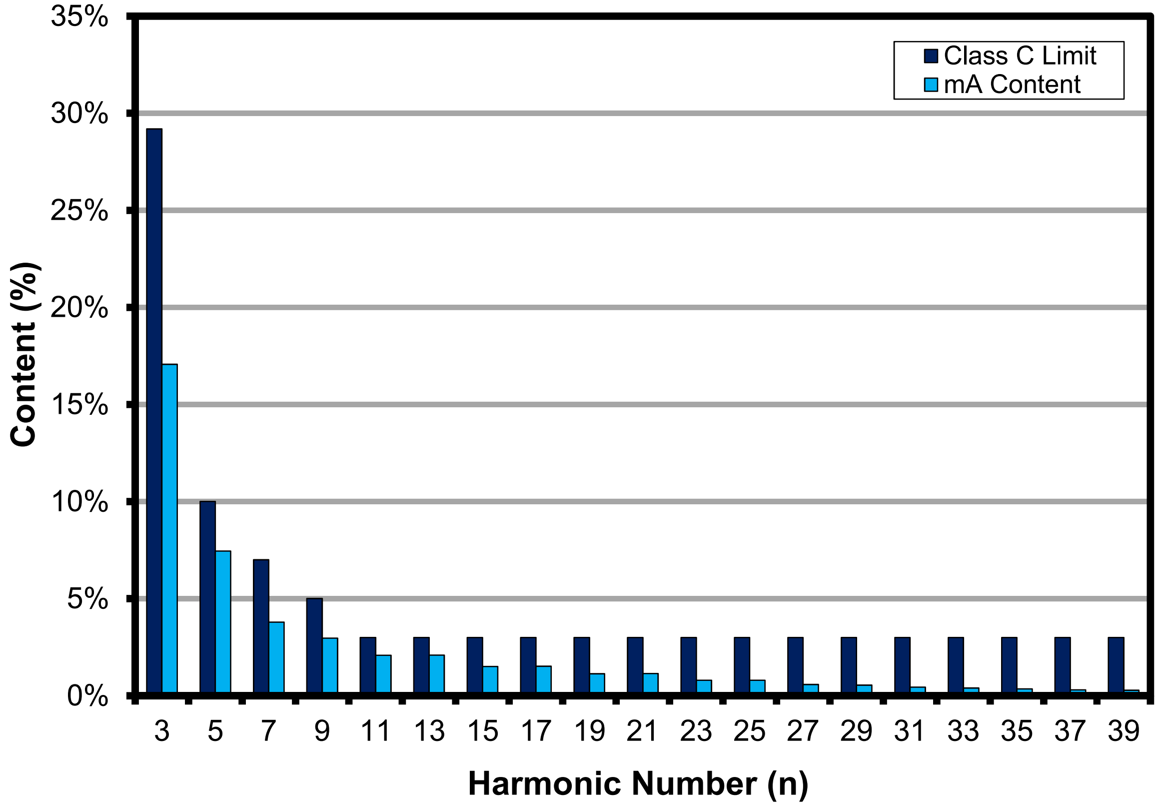

Figure 15 – Two 50 V LED Loads Input Current Harmonics at 230 VAC, 50 Hz of Two Drivers in Parallel.

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11.6 Test Data

All measurements were taken with the board at open frame, 25 °C ambient, and 50 Hz line frequency.

11.6.1 Test Data, 48 V LED Load

Input		Input Measurement					Load Measurement			Calculation		
VAC (V_{RMS})	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	P_{CAL} (W)	Efficiency (%)	Loss (W)
180	50	180.01	138.01	24.389	0.982	17.63	48.2900	437	21.180	21.08	86.84	3.21
200	50	200.00	125.60	24.591	0.979	18.38	48.3000	441	21.410	21.30	87.06	3.18
220	50	220.00	114.90	24.656	0.975	19.18	48.3000	443	21.480	21.38	87.12	3.18
230	50	230.04	110.02	24.627	0.973	19.66	48.2900	442	21.460	21.36	87.14	3.17
265	50	265.05	95.55	24.383	0.963	21.63	48.2600	438	21.220	21.13	87.03	3.16

11.6.2 Test Data, 50 V LED Load

Input		Input Measurement					Load Measurement			Calculation		
VAC (V_{RMS})	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	P_{CAL} (W)	Efficiency (%)	Loss (W)
180	50	179.99	141.55	25.025	0.982	17.46	49.7100	435	21.730	21.64	86.83	3.30
200	50	199.99	128.81	25.234	0.980	18.2	49.7200	440	21.970	21.87	87.07	3.26
220	50	219.99	117.83	25.299	0.976	19.07	49.7200	442	22.050	21.95	87.16	3.25
230	50	230.02	112.85	25.279	0.974	19.52	49.7000	441	22.030	21.94	87.15	3.25
265	50	265.04	97.99	25.033	0.964	21.64	49.6700	437	21.800	21.71	87.09	3.23

11.6.3 Test Data, 52 V LED Load

Input		Input Measurement					Load Measurement			Calculation		
VAC (V_{RMS})	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	P_{CAL} (W)	Efficiency (%)	Loss (W)
180	50	180.01	147.09	26.026	0.983	17.14	51.9600	433	22.600	22.50	86.84	3.43
200	50	200.00	133.88	26.252	0.980	17.87	51.9700	438	22.860	22.76	87.08	3.39
220	50	220.00	122.43	26.315	0.977	18.72	51.9700	440	22.950	22.86	87.21	3.37
230	50	230.04	117.17	26.278	0.975	19.19	51.9500	439	22.920	22.83	87.22	3.36
265	50	265.05	101.73	26.027	0.965	21.31	51.9100	435	22.680	22.60	87.14	3.35

11.6.4 230 VAC 50 Hz, 48 V LED Load Harmonics Data

V	Freq	I (mA)	P	PF	%THD
230	50.00	110.02	24.6270	0.9731	19.66
nth Order	**mA Content**	**% Content**	**Limit >25 W**	**Remarks**	
1	107.83				
2	0.08	0.07%	2.00%		
3	18.46	17.12%	29.19%	Pass	
5	8.04	7.46%	10.00%	Pass	
7	3.95	3.66%	7.00%	Pass	
9	2.89	2.68%	5.00%	Pass	
11	1.83	1.70%	3.00%	Pass	
13	2.11	1.96%	3.00%	Pass	
15	1.96	1.82%	3.00%	Pass	
17	1.57	1.46%	3.00%	Pass	
19	1.09	1.01%	3.00%	Pass	
21	1.07	0.99%	3.00%	Pass	
23	0.81	0.75%	3.00%	Pass	
25	0.86	0.80%	3.00%	Pass	
27	0.60	0.56%	3.00%	Pass	
29	0.61	0.57%	3.00%	Pass	
31	0.47	0.44%	3.00%	Pass	
33	0.45	0.42%	3.00%	Pass	
35	0.34	0.32%	3.00%	Pass	
37	0.33	0.31%	3.00%	Pass	
39	0.31	0.29%	3.00%	Pass	

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11.6.5 230 VAC 50 Hz, 50 V LED Load Harmonics Data

V	Freq	I (mA)	P	PF	%THD
230	50.00	112.85	25.2790	0.9738	19.52
nth Order	**mA Content**	**% Content**	**Limit >25 W**	**Remarks**	
1	110.60				
2	0.10	0.09%	2.00%		
3	18.82	17.02%	29.21%	Pass	
5	8.13	7.35%	10.00%	Pass	
7	3.98	3.60%	7.00%	Pass	
9	2.92	2.64%	5.00%	Pass	
11	1.88	1.70%	3.00%	Pass	
13	1.96	1.77%	3.00%	Pass	
15	2.42	2.19%	3.00%	Pass	
17	1.44	1.30%	3.00%	Pass	
19	1.05	0.95%	3.00%	Pass	
21	1.11	1.00%	3.00%	Pass	
23	0.82	0.74%	3.00%	Pass	
25	0.85	0.77%	3.00%	Pass	
27	0.62	0.56%	3.00%	Pass	
29	0.61	0.55%	3.00%	Pass	
31	0.45	0.41%	3.00%	Pass	
33	0.44	0.40%	3.00%	Pass	
35	0.35	0.32%	3.00%	Pass	
37	0.33	0.30%	3.00%	Pass	
39	0.27	0.24%	3.00%	Pass	

11.6.6 230 VAC 50 Hz, 52 V LED Load Harmonics Data

V	Freq	I (mA)	P	PF	%THD
230	50.00	117.17	26.2780	0.9749	19.19
nth Order	**mA Content**	**% Content**	**Limit >25 W**	**Remarks**	
1	114.88				
2	0.08	0.07%	2.00%		
3	19.30	16.80%	29.25%	Pass	
5	8.26	7.19%	10.00%	Pass	
7	4.06	3.53%	7.00%	Pass	
9	2.96	2.58%	5.00%	Pass	
11	1.87	1.63%	3.00%	Pass	
13	1.60	1.39%	3.00%	Pass	
15	2.50	2.18%	3.00%	Pass	
17	1.49	1.30%	3.00%	Pass	
19	1.09	0.95%	3.00%	Pass	
21	1.12	0.97%	3.00%	Pass	
23	0.79	0.69%	3.00%	Pass	
25	0.78	0.68%	3.00%	Pass	
27	0.57	0.50%	3.00%	Pass	
29	0.57	0.50%	3.00%	Pass	
31	0.43	0.37%	3.00%	Pass	
33	0.40	0.35%	3.00%	Pass	
35	0.33	0.29%	3.00%	Pass	
37	0.32	0.28%	3.00%	Pass	
39	0.29	0.25%	3.00%	Pass	

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12 Thermal Performance

Images captured after running for >30 minutes at room temperature (25 °C), open frame for the conditions specified.

12.1 V_{IN} = 230 VAC, 50 Hz, 50 V LED Load

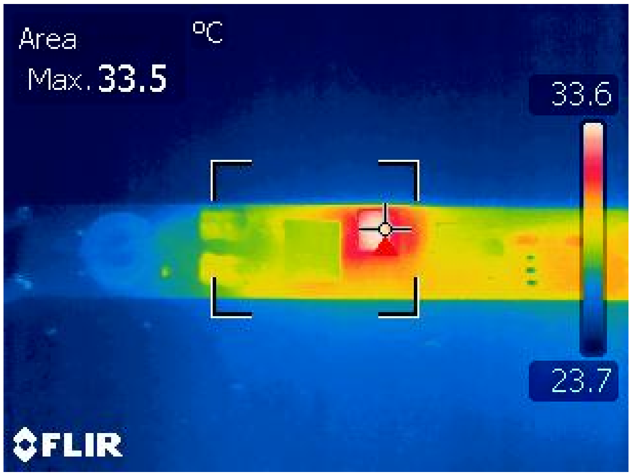

Figure 16 – Input Area. 230 VAC, 50 Hz.

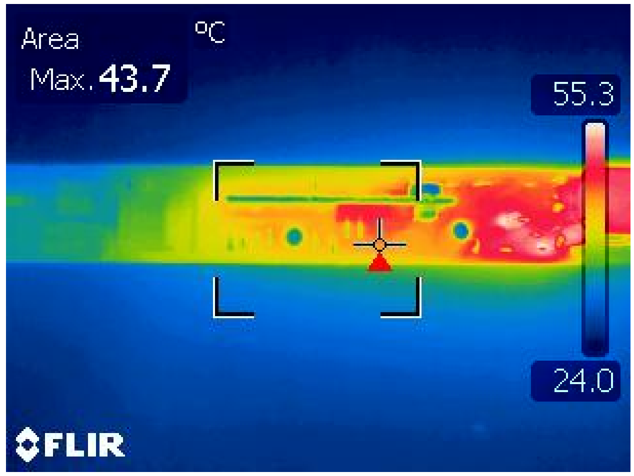

Figure 17 – LNK419EG Area. 230 VAC, 50 Hz.

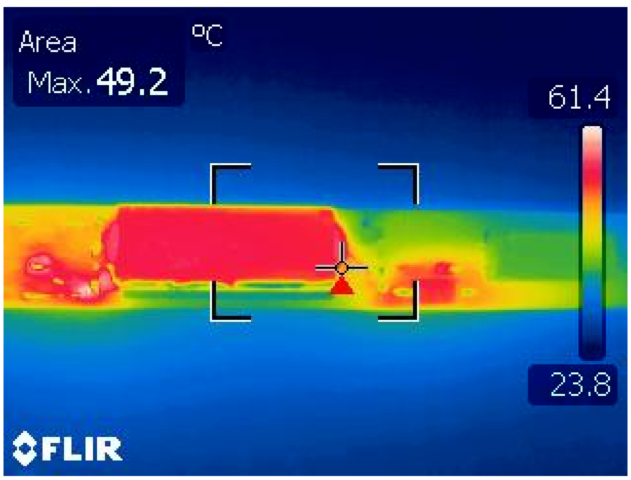

Figure 18 – Transformer and Output Area. 230 VAC, 50 Hz.

13 Waveforms

13.1 Input Voltage and Input Current Waveforms

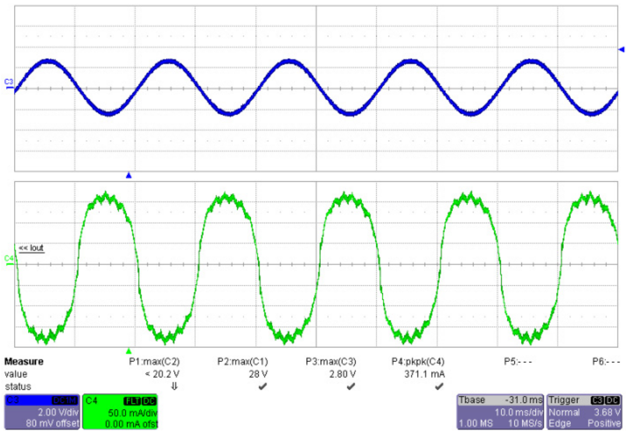

Figure 19 – 180 VAC, Full Load.
Upper: V_{IN}, 200 V / div.
Lower: I_{IN}, 50 mA, 10 ms / div.

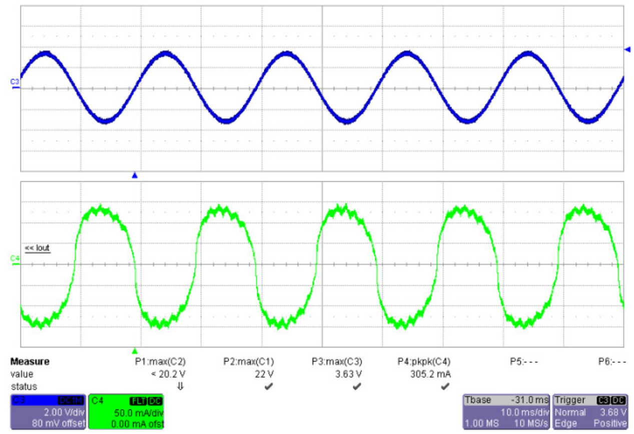

Figure 20 – 230 VAC, Full Load.
Upper: V_{IN}, 200 V / div.
Lower: I_{IN}, 50 mA, 10 ms / div.

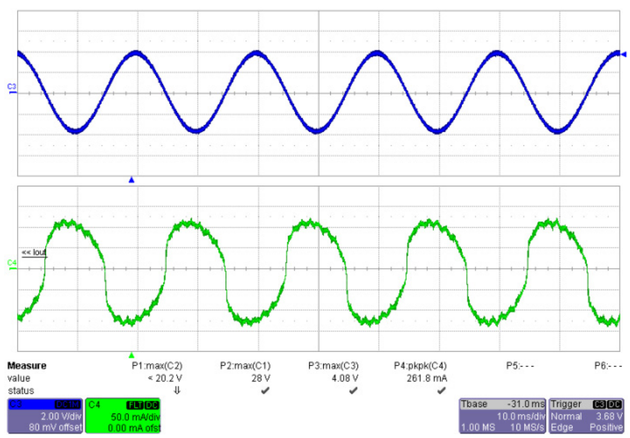

Figure 21 – 265 VAC, Full Load.
Upper: V_{IN}, 200 V / div.
Lower: I_{IN}, 50 mA, 10 ms / div.

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13.2 Output Voltage and Output Current Waveforms

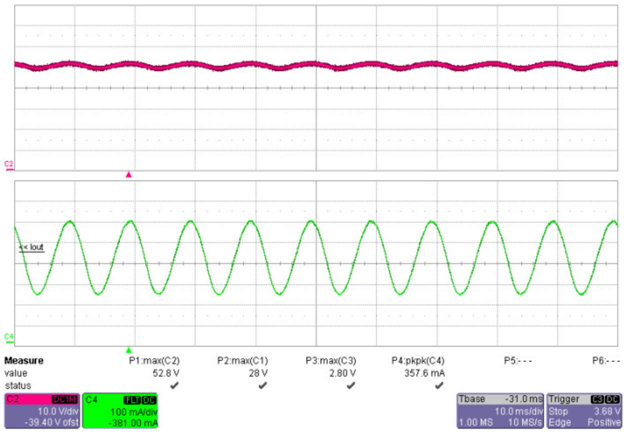

Figure 22 – 180 VAC, 50 Hz Full Load.
Upper: V_{OUT}, 10 V / div.
Lower: I_{OUT}, 100 mA, 10 ms / div.

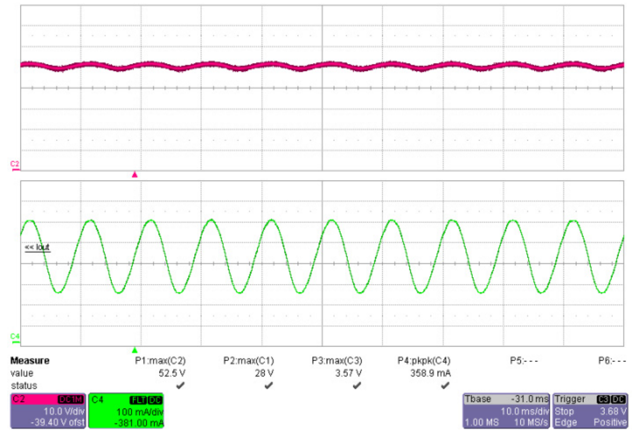

Figure 23 – 230 VAC, 50 Hz Full Load.
Upper: V_{OUT}, 10 V / div.
Lower: I_{OUT}, 100 mA, 10 ms / div.

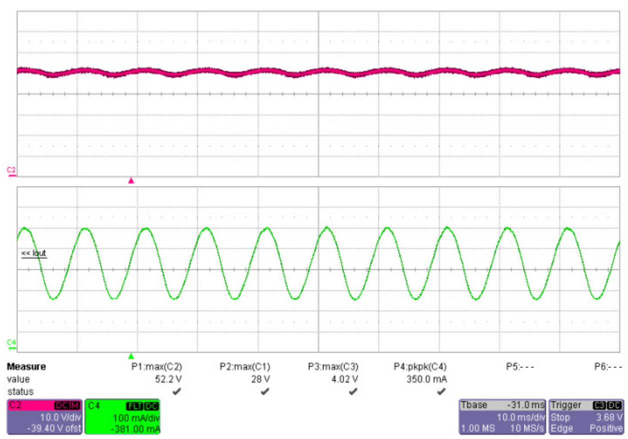

Figure 24 – 265 VAC, 50 Hz Full Load.
Upper: V_{OUT}, 10 V / div.
Lower: I_{OUT}, 100 mA, 10 ms / div.

13.3 Output Voltage and Output Current Waveforms at Start-up

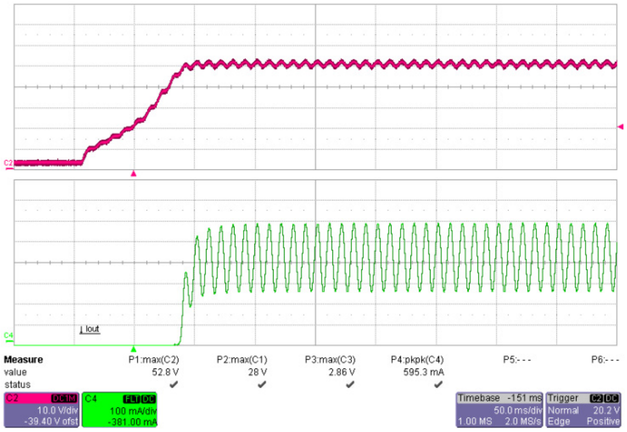

Figure 25 – 180 VAC Output Rise.
Upper: V_{OUT}, 10 V / div.
Lower: I_{OUT}, 100 mA, 50 ms / div.

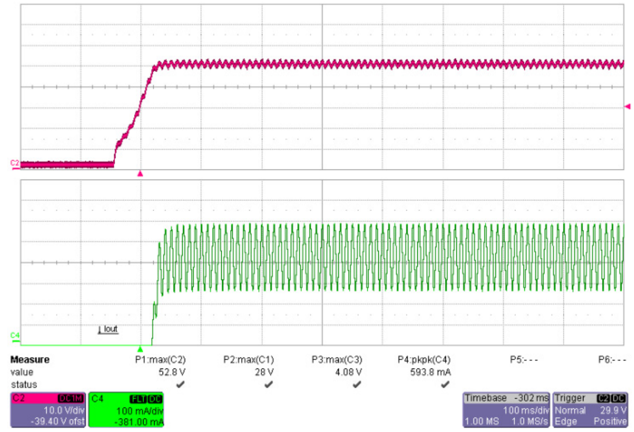

Figure 26 – 265 VAC Output Fall.
Upper: V_{OUT}, 10 V / div.
Lower: I_{OUT}, 100 mA, 100 ms / div.

13.4 Drain Voltage and Current Waveforms at Start-up

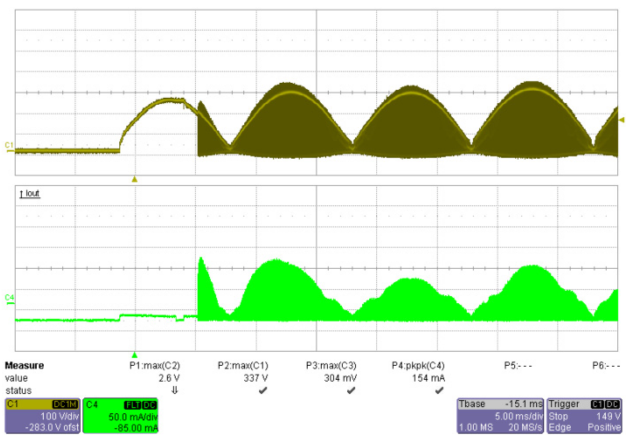

Figure 27 – 180 VAC, 50 Hz Start-up.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 50 mA, 5 ms / div.

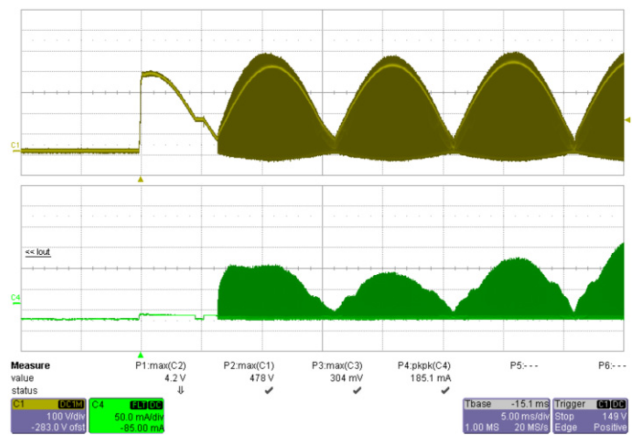

Figure 28 – 265 VAC, 50 Hz Start-up.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 50 mA, 5 ms / div.

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13.5 Input Voltage and Output Current Waveforms at Start-up

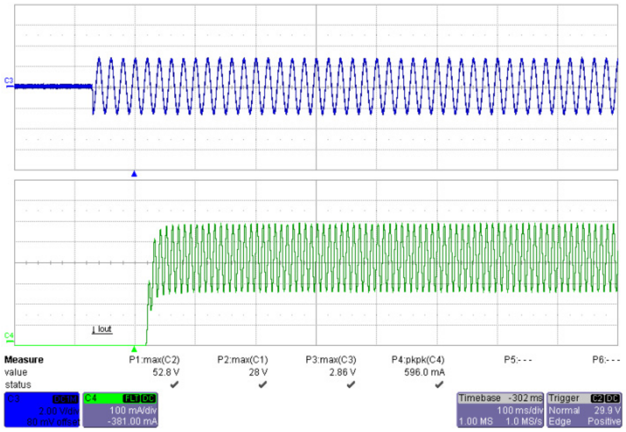

Figure 29 – 180 VAC, 50 Hz.
Upper: V_{IN}, 200 V / div.
Lower: I_{OUT}, 100 mA, 100 ms / div.

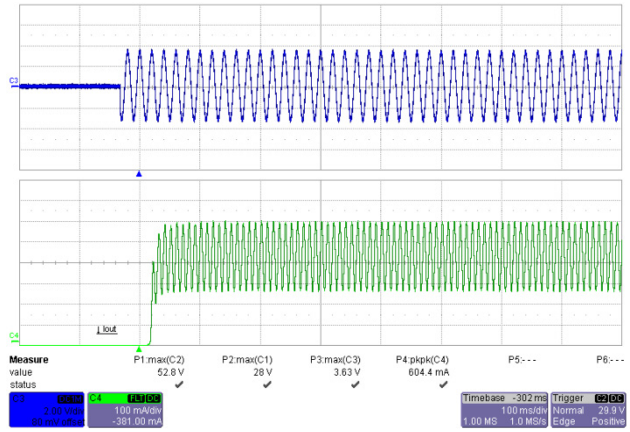

Figure 30 – 230 VAC, 50 Hz.
Upper: V_{IN}, 200 V / div.
Lower: I_{OUT}, 100 mA, 100 ms / div.

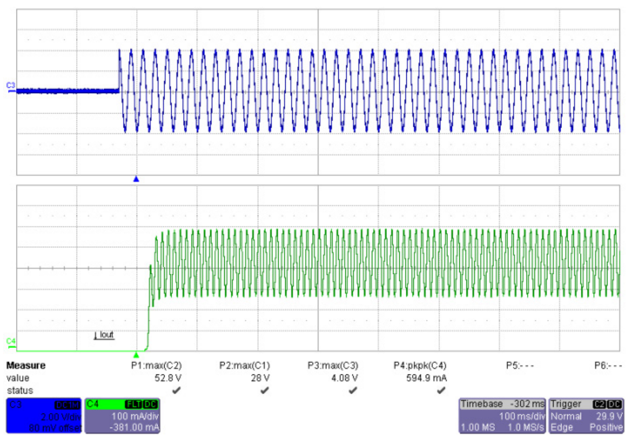

Figure 31 – 265 VAC, 50 Hz.
Upper: V_{IN}, 200 V / div.
Lower: I_{OUT}, 100 mA, 100 ms / div.

13.6 Drain Voltage and Current Waveforms

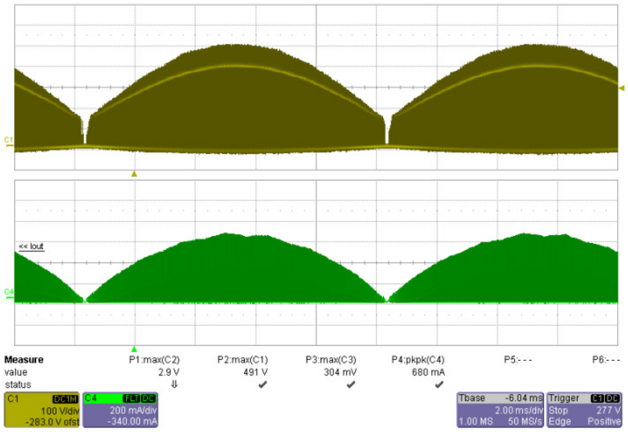

Figure 32 – 180 VAC, 50 Hz.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 200 mA, 2 ms / div.

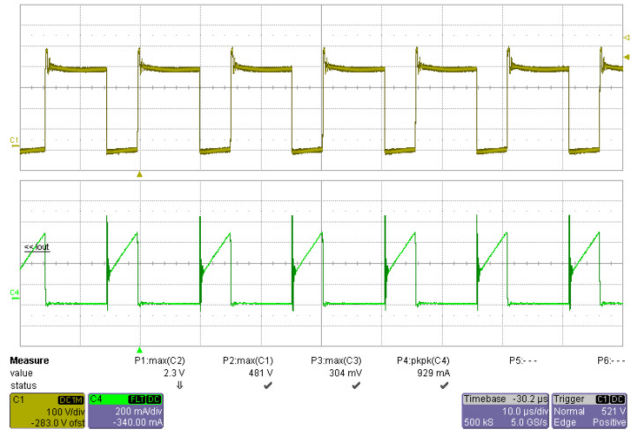

Figure 33 – 180 VAC, 50 Hz.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 200 mA, 10 us / div.

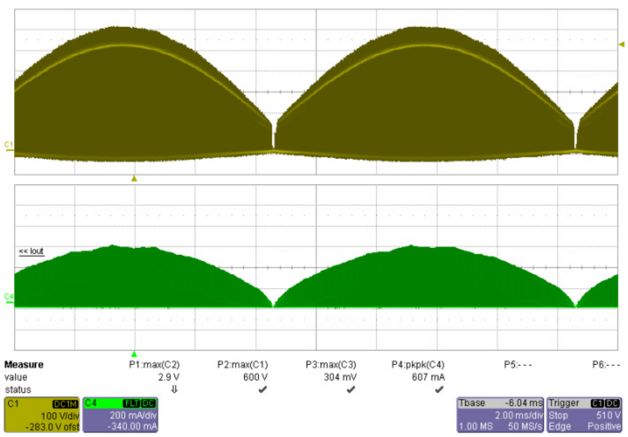

Figure 34 – 265 VAC, 50 Hz.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 200 mA, 2 ms / div.

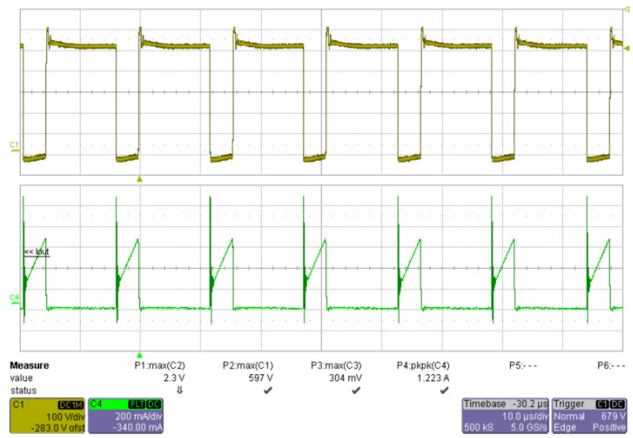

Figure 35 – 265 VAC, 50 Hz.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 200 mA, 10 us / div.

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13.7 Output Short Condition

During output short condition, the I_{FB} current falls below the $I_{FB(AR)}$ threshold and enters the auto-restart condition. During this condition, to minimize power dissipation on the power components, the auto-restart circuit turns the power supply on and off at an auto-restart duty cycle of typically DC_{AR} for as long as the fault condition persists.

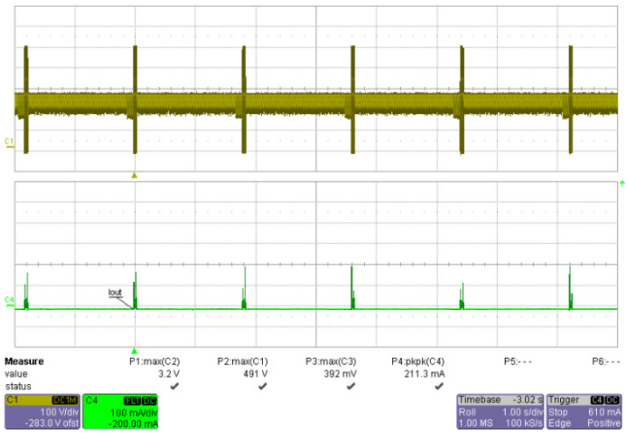

Figure 36 – 180 VAC, 50 Hz Output Short Condition.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 100 mA, 1 s / div.

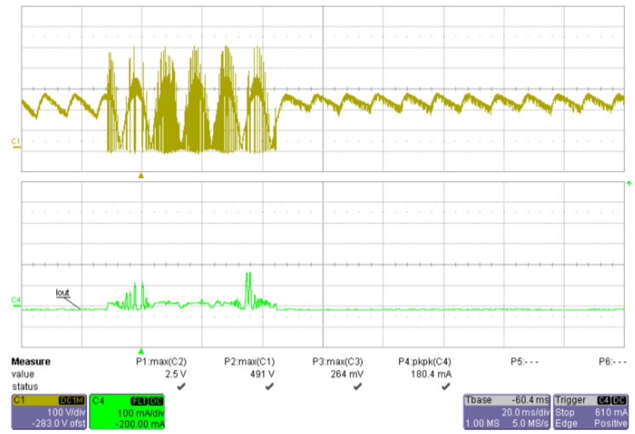

Figure 37 – 180 VAC, 50 Hz Output Short Condition.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 100 mA, 20 ms / div.

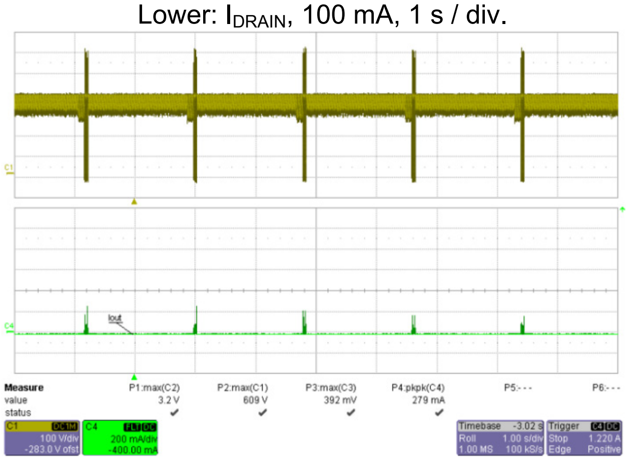

Figure 38 – 265 VAC, 50 Hz Output Short Condition.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 200 mA, 1 s / div.

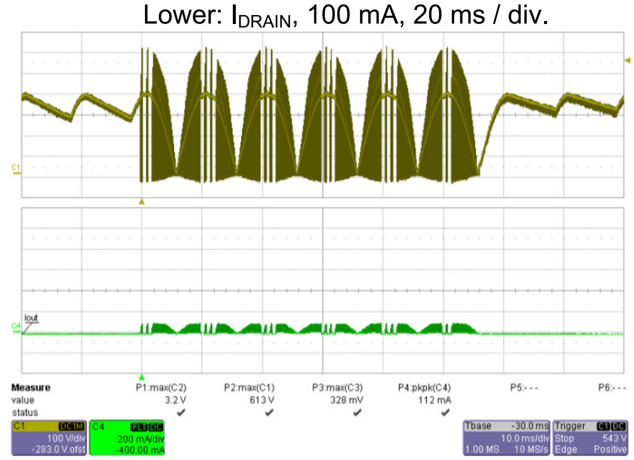

Figure 39 – 265 VAC, 50 Hz Output Short Condition.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 200 mA, 10 ms / div.

13.8 Output Diode Voltage and Current Waveforms

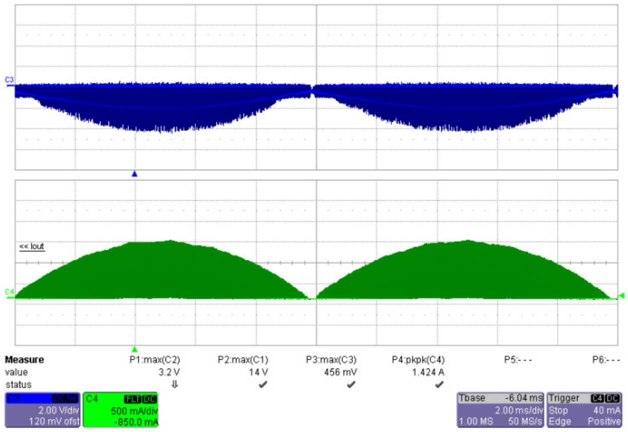

Figure 40 – 265 VAC, 50 Hz Normal Operation.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 500 mA, 2 ms / div.

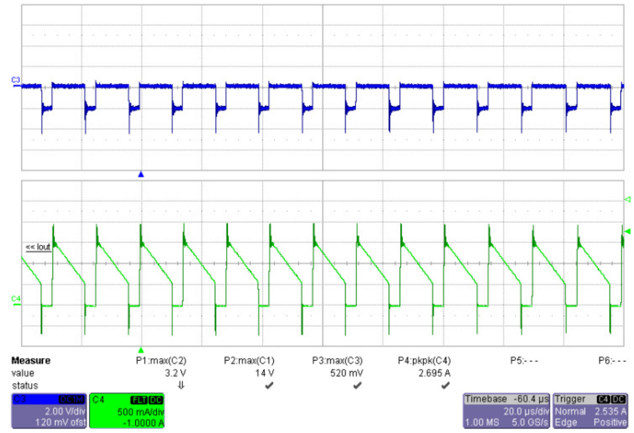

Figure 41 – 265 VAC, 50 Hz Output Short.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 500 mA, 20 us / div.

13.9 Output Voltage Waveforms at Open Load

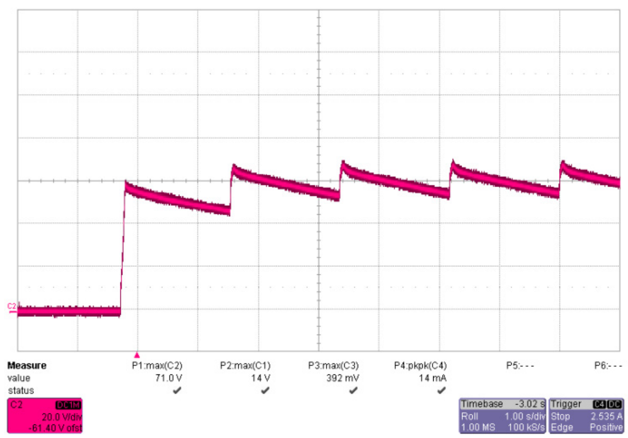

Figure 42 – 265 VAC, 50 Hz Output Open.
$V_{OUT,}$ 20 V / div, 1 s/div.

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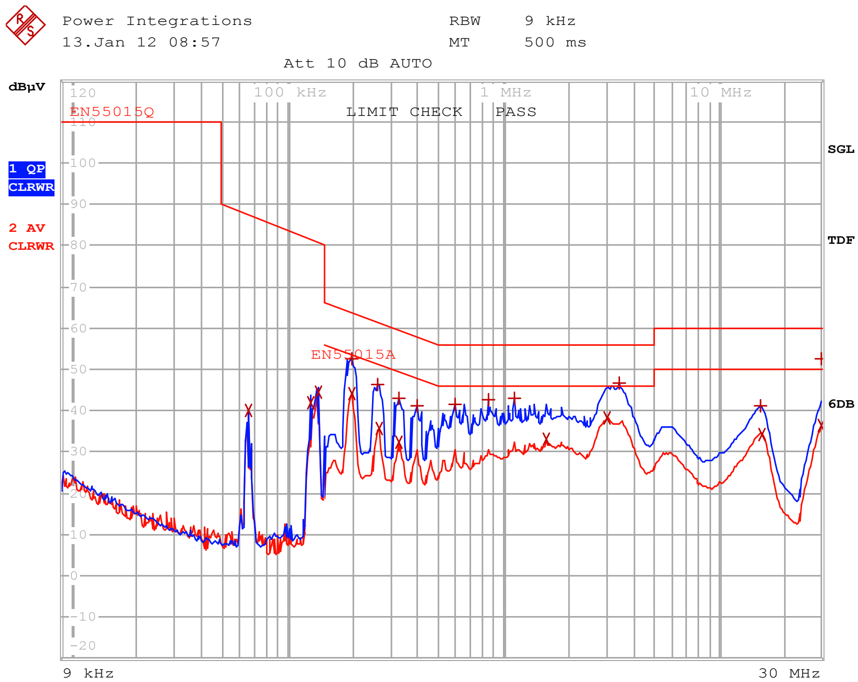
14 Conducted EMI



EDIT PEAK LIST (Final Measurement Results)		
Trace1:	EN55015Q	
Trace2:	EN55015A	
Trace3:	---	

TRACE		FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
2	Average	65.8441606665 kHz	39.94	L1 gnd	
2	Average	128.247618558 kHz	41.99	N gnd	
2	Average	137.49880568 kHz	44.31	N gnd	
1	Quasi Peak	196.231331718 kHz	52.56	L1 gnd	-11.20
2	Average	198.193645035 kHz	44.16	L1 gnd	-9.52
1	Quasi Peak	261.871472881 kHz	46.41	L1 gnd	-14.95
2	Average	264.49018761 kHz	35.52	L1 gnd	-15.76
1	Quasi Peak	329.215131266 kHz	43.06	L1 gnd	-16.40
2	Average	329.215131266 kHz	32.47	L1 gnd	-16.99
1	Quasi Peak	393.789848222 kHz	41.08	L1 gnd	-16.89
1	Quasi Peak	592.16241791 kHz	41.62	L1 gnd	-14.37
1	Quasi Peak	855.719977385 kHz	42.66	L1 gnd	-13.34
1	Quasi Peak	1.1194604716 MHz	43.17	N gnd	-12.82
2	Average	1.58583078933 MHz	33.14	N gnd	-12.85
2	Average	3.02793216507 MHz	38.26	L1 gnd	-7.73
1	Quasi Peak	3.44606925067 MHz	46.74	L1 gnd	-9.25
1	Quasi Peak	15.6376977805 MHz	41.12	L1 gnd	-18.87
2	Average	15.7940747583 MHz	34.37	L1 gnd	-15.62
1	Quasi Peak	30 MHz	52.65	L1 gnd	-7.34
2	Average	30 MHz	36.22	L1 gnd	-13.77

Figure 43 – Conducted EMI, 50 V LED Load, 230 VAC, 50 Hz -Line, and EN55015 B Limits**.**

EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55015Q
Trace2: EN55015A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
2	Average	64.5467705779 kHz	36.39	L1 gnd	
2	Average	65.8441606665 kHz	39.93	L1 gnd	
2	Average	126.977840157 kHz	42.78	N gnd	
2	Average	137.49880568 kHz	45.33	L1 gnd	
1	Quasi Peak	196.231331718 kHz	52.51	L1 gnd	-11.25
1	Quasi Peak	198.193645035 kHz	52.49	L1 gnd	-11.19
2	Average	198.193645035 kHz	44.09	L1 gnd	-9.59
1	Quasi Peak	261.871472881 kHz	46.41	L1 gnd	-14.95
2	Average	264.49018761 kHz	35.47	L1 gnd	-15.81
1	Quasi Peak	329.215131266 kHz	43.08	L1 gnd	-16.38
2	Average	329.215131266 kHz	32.51	L1 gnd	-16.95
1	Quasi Peak	393.789848222 kHz	40.90	L1 gnd	-17.07
1	Quasi Peak	592.16241791 kHz	41.65	L1 gnd	-14.34
1	Quasi Peak	855.719977385 kHz	42.60	L1 gnd	-13.39
1	Quasi Peak	1.1194604716 MHz	43.04	N gnd	-12.95
2	Average	1.58583078933 MHz	33.09	N gnd	-12.90
1	Quasi Peak	3.44606925067 MHz	46.61	L1 gnd	-9.38
2	Average	3.58599348099 MHz	37.07	L1 gnd	-8.92
1	Quasi Peak	15.6376977805 MHz	41.15	L1 gnd	-18.85
2	Average	15.6376977805 MHz	34.48	L1 gnd	-15.51

Figure 44 – Conducted EMI, 50 V LED Load, 230 VAC, 50 Hz- Neutral, and EN55015 B Limits**.**

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15 Line Surge

The unit was subjected to 2500 V ring wave and 1000 V differential surge at 230 VAC using 10 strikes at each condition. A test failure was defined as a non-recoverable interruption of output requiring supply repair or recycling of input voltage.

Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Type	Test Result (Pass/Fail)
+2500	230	L1, L2	0	100 kHz Ring Wave (500 A)	Pass
-2500	230	L1, L2	0	100 kHz Ring Wave (500 A)	Pass
+2500	230	L1, L2	90	100 kHz Ring Wave (500 A)	Pass
-2500	230	L1, L2	90	100 kHz Ring Wave (500 A)	Pass

Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Type	Test Result (Pass/Fail)
+1000	230	L1, L2	0	Surge (2Ω)	Pass
-1000	230	L1, L2	0	Surge (2Ω)	Pass
+1000	230	L1, L2	90	Surge (2Ω)	Pass
-1000	230	L1, L2	90	Surge (2Ω)	Pass

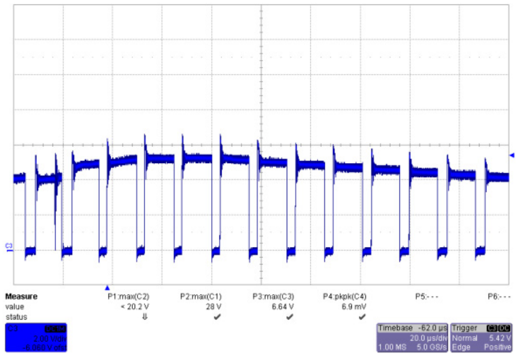

Figure 45 – 1 kV Differential Surge.
V_{DRAIN}, 200 V / div., 20 us / div.

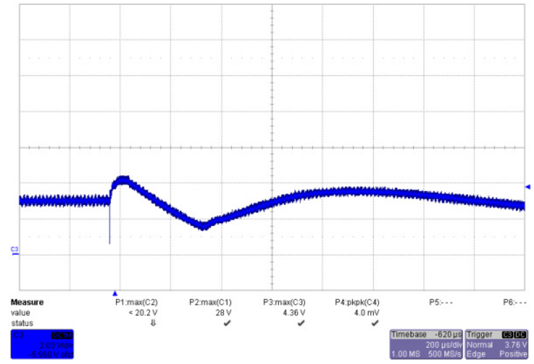

Figure 46 – 1 kV Differential Surge.
V_{BUS}, 200 V / div., 200 us / div.

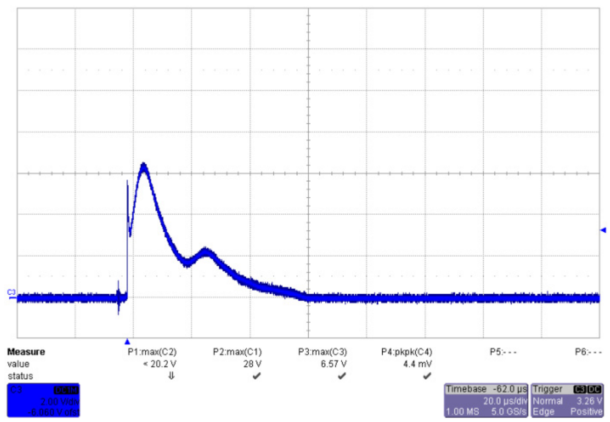

Figure 47 – 1 kV Differential Surge.
V_R, 200 V / div., 20 us / div.

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16 Revision History

Date	Author	Revision	Description and Changes	Reviewed
07-Mar-12	DK	1.0	Initial Release	Apps & Mktg

For the latest updates, visit our website: www.powerint.com

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