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Issue 1

SIGNAL-INTEGRITY ISSUES ON THE RISE

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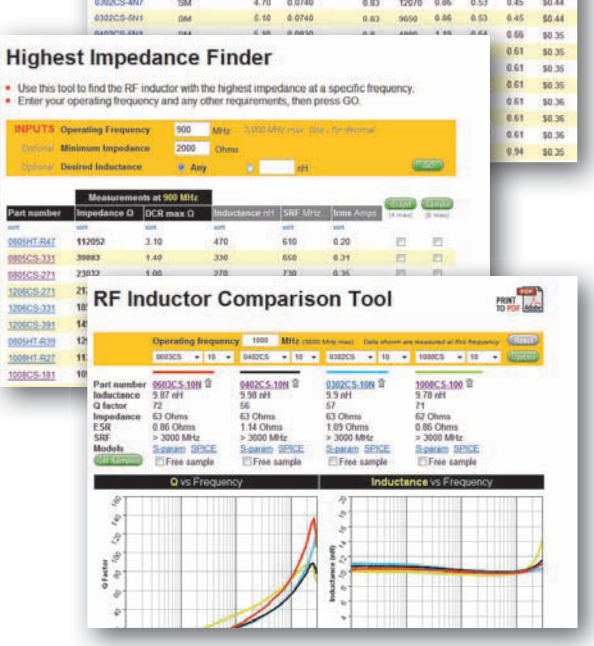
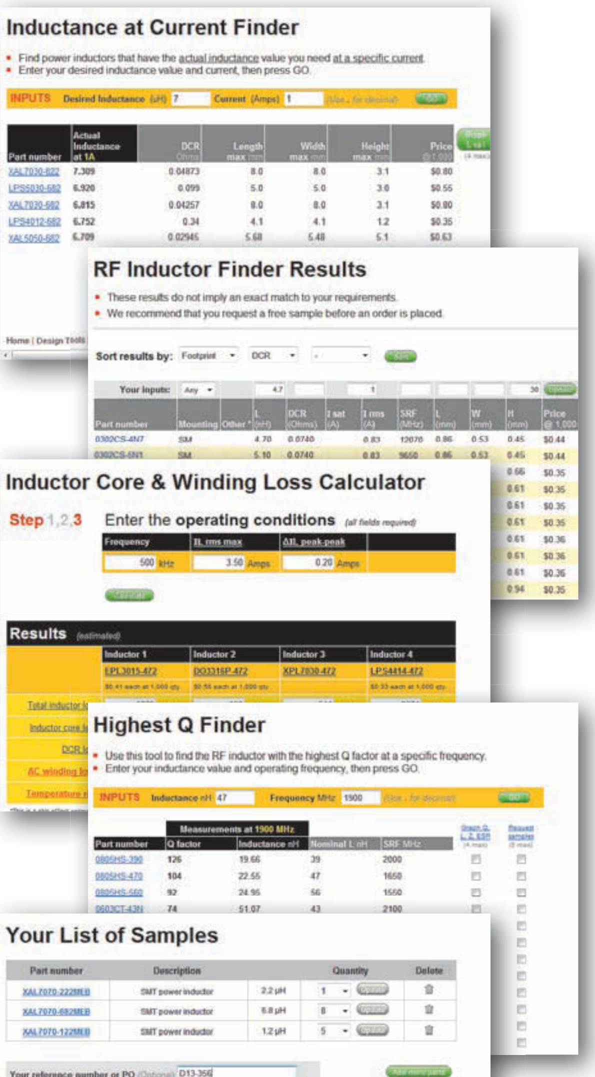

Highest Impedance Finder
Use this tool to find the RF inductor with the highest impedance at a specific frequency.
Enter your operating frequency and any other requirements, then press GO.
RF Inductor Comparison Tool
Q vs Frequency
Inductance vs Frequency


Inductance at Current Finder
Find power inductors that have the actual inductance value you need at a specific current.
Enter your desired inductance value and current, then press GO.
RF Inductor Finder Results
These results do not imply an exact match to your requirements.
We recommend that you request a free sample before an order is placed.
Inductor Core & Winding Loss Calculator
Step 1,2,3 Enter the operating conditions
Results
Highest Q Finder
Use this tool to find the RF inductor with the highest Q factor at a specific frequency.
Enter your inductance value and operating frequency, then press GO.
Your List of Samples


AT&T
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Power Inductor Selection Tools
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Datasheets
THE WORLD'S MOST POWERFUL
MAGNETIC FIELD

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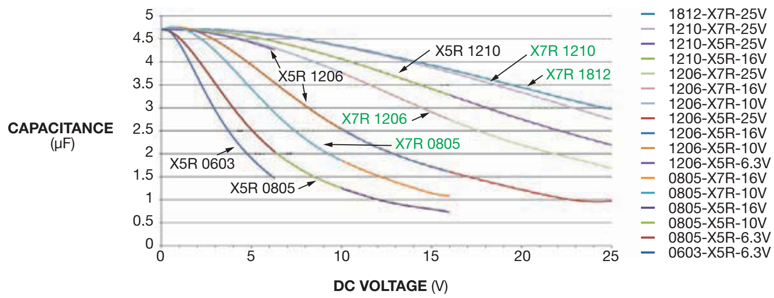
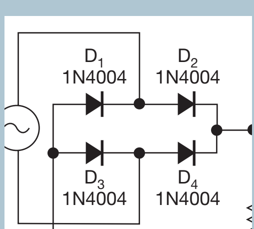


IMAGE(S): SHUTTERSTOCK

DESIGNIDEAS



▶ Find out how to submit your own Design Idea: www.edn.com/4394666.

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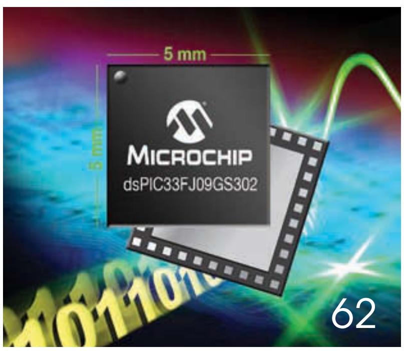
pulse

DEPARTMENTS & COLUMNS



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EDN online

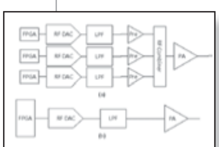
JOIN THE CONVERSATION

Comments, thoughts, and opinions shared by *EDN*'s community

In response to "Next round: GaN versus Si," a post in the Dave's Power Trips blog at www.edn.com/4403311, UncommonTruthiness commented:

Material	Bandgap (Eg) (eV)	Electron Mobility (cm²/V-sec)	Intrinsic Carrier Concentration (ni) @ 300°C (cm⁻³)	Critical Field 10⁶ (Ec) (V/cm)	Saturated Electron Drift Velocity (cm/s) (Vs)
Silicon (Si)	1.1	1450	>1.0 x 10^{15}	0.25	1.0 x 10^7
Silicon Carbide (SiC)	3.26	900	1.0 x 10^4	2.2	2.0 x 10^7
Gallium Nitride (GaN)	3.2	2000	2.0 x 10^2	3	2.5.0 x 10^7

"The battleground will be substrate price. At ~$5,000 for a 150-mm GaN/Si substrate and $3,000 for a 100-mm SiC substrate + epi, it will take a very special device to command an ASP [average selling price] that will yield a return on that direct cost. This motivates a market segment dominated by military, aerospace, and perhaps medical applications. Vertical integration in the manufacturing of GaN/Si at the device manufacturer can reduce that cost by perhaps as much as 10 times, which would improve available market opportunities. I don't see such a cost-reduction opportunity for SiC, which could be a major limiter for SiC materials' ability to address commodity markets."



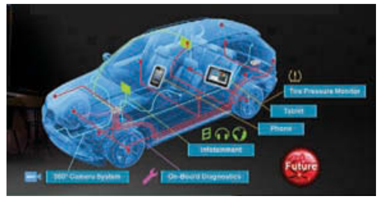
In response to "RF DACs simplify power and space in downstream cable transmitter systems," an article by Daniel E Fague and Sara Nadeau at www.edn.com/4403455, WKetel commented:

"Perhaps it may seem to be of a more 'luddite' orientation, but perhaps we really don't need all of these additional broadband functions. Just possibly there should be some technical limitation on the amount of advertising that can be carried at any given instant. Of course, the ultrahigh performance of the newest RF DAC is quite impressive, but we may actually be better off without it. Just because we can does not mean that we should."

EDN *invites all of its readers to comment constructively and creatively on our content. You'll find the opportunity to do so at the bottom of each article and blog post.*

CONTENT

Can't-miss content on EDN.com

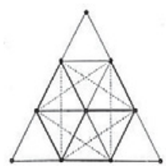


THE CONNECTED CAR AS A PLATFORM

When people think of the connected car, they think of a car that hooks to the cloud. The reality is that the car itself is a connected platform that enables multiple protocols to talk together and connects to the cloud through the occupant's mobile cellular service and hardware.

www.edn.com/4403736

MATHEMATICS OF SOUND



Almost every sound we hear comprises rich harmonics—overtones that we may not notice, but that are essential in producing the timbre and the meaning of sound—and math fits into all of it.

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ACE AWARDS NOMINATIONS NOW OPEN

Get ready to shine! *EDN* and *EE Times* have opened the call for nominations for the 2013 ACE Awards competition, in which we'll honor the people and technologies that have made a difference in the electronics industry in the last year. To claim your share of the glory or give a thumbs-up to someone else's work, make your nominations for the ACE Awards before Feb 1, 2013, here: http://ubm-ace.com.

BY PATRICK MANNION, BRAND DIRECTOR

Mind of the Engineer: rational versus emotional?

At DesignCon later this month, *EE Times* brand director Alex Wolfe and I will host a breakfast to present the results of the first ever cross-brand, global version of an *EDN* classic: "The Mind of the Engineer" study. We'll condense the results of the sweeping study, which endeavors to tell you all about you: who you are; what you like; how you see yourself; how you think others see you; your concerns, worries, and fears; what makes you happy; what inspires you; how you view your peers; and, of course, your ambitions, goals, and the resources you depend upon to get you there. This year, we've even grouped you according to four main personas: Big Man on Campus; Salt of the Earth; New da Vinci; and the Quiet One. Come join us to find out where you fit.

It's all very intriguing—after all, we all love to hear about ourselves—but is this really the mind of the engineer? I wonder about that.

A while back, my son gave me a riddle to solve. I started to ask questions, break it down, define the parameters and conditions, and generally pester him until he broke down and yelped, "Dad, you're overanalyzing again; stop it!"

He was right; I do tend to overanalyze. That's why I found the book *How We Decide*, by Jonah Lehrer, so intriguing. Lehrer is a Rhodes Scholar and all-around smart guy who knows a lot about how the brain works, yet even he admits to having made two wrong decisions that later got him fired.

Lehrer's exploration of human decision-making starts with a look at New England Patriots quarterback Tom Brady. Lehrer notes how hard it is to break down what Brady does in real time at clutch moments on the field; during such moments, the subconscious takes over, and things just happen.

How does that process unfold? Can it be applied elsewhere? The answer is yes, but it requires the decision-maker to do something engineers are taught not to do.

In his book, Lehrer guides us on a journey through the writings of Plato to Freud and on to current-day cognitive psychology, all of which support what he calls "the privileging of reason over emotion." Emotions, these writings tell us, are bad impulses that should be controlled and suppressed, lest they get in the way of rational thought and good decision-making.

But then Lehrer relates the story of a patient he calls Elliott who lost the ability to make a decision after having a part of his brain removed to excise a tumor. In short, the surgery killed Elliott's ability to "feel," leaving him completely rational yet also completely unable to make a decision.

Why was that?

In engineering school, we're taught the importance of rational thinking. In fact, for many engineers, it's the affinity for the "rational" that attracts them to the field in the first place. But Lehrer notes that Elliott's inability to make a decision came down to lack of emotion. To make good decisions, we must learn to combine rational thought with emotional awareness. We've heard this before when we've been advised to follow our gut or trust our instincts.

Malcolm Gladwell, the consummate observer of human nature, points out in his book *Blink* that generals in the field make life-and-death decisions all the time in situations where they have only 60% or so of the information required. They are able to do so because they are attuned to their gut instincts, or "feelings" (gag)—which, according to Lehrer and other experts, we generate subconsciously, based on our prior experiences and accumulated knowledge.

The ability to make wise decisions requires the decision-maker to do something engineers are taught not to do: heed their emotions.

These fascinating findings underscore the importance of combining rational thought with instinct to make the right decisions for your design. Your emotions are telling you something, so listen up. Got that nagging sense something is wrong? Don't act until you find out the cause.

In the meantime, if you tire of thinking about you, you can find out what others think of you by joining Alex, myself, and the UBM Tech team on Wednesday, Jan 30, in the Santa Clara Convention Center, Room M3. You'll also find me at the relaunch party for *Planet Analog* later that day, at 6 pm, in the Mission City Ballroom, Showroom 3.

I look forward to seeing you. **EDN**

Contact me at patrick.mannion@ubm.com.


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INNOVATIONS & INNOVATORS

Tektronix unveils entry-level oscilloscopes

With prices starting at $520, the TBS1000 series of digital storage oscilloscopes from Tektronix offers engineers, educators, and hobbyists an affordable tool for a variety of general-purpose electronics test applications. Each of the five models in the entry-level series provides two analog channels, a record length of 2500 points across all time bases, 16 automated waveform measurements, an external trigger input, and a 5.7-in. color TFT LCD.

The TBS1000 series gives users a choice of bandwidths, with sampling rates of 500M samples/sec for the 25- and 40-MHz scopes and 1G sample/sec for the 60-, 100-, and 150-MHz scopes. On all models, dc vertical accuracy is ±3%, for accurate measurements on even low-level signals. Vertical sensitivity ranges from 2 mV to 5V/div with calibrated fine adjustment.

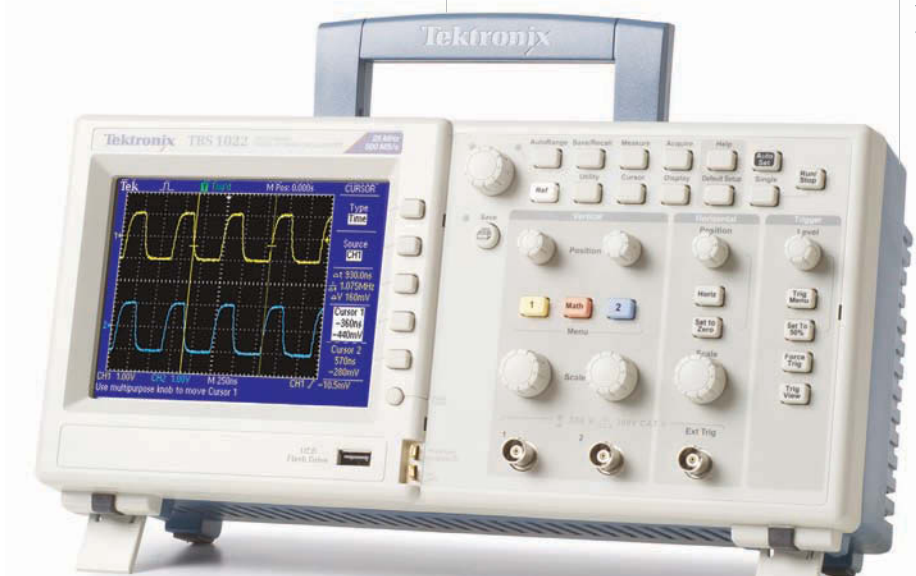
Automatic waveform measurements calculate important signal characteristics, including period, frequency, positive and negative pulse width, rise and fall time, maximum, minimum, peak-to-peak, mean, RMS, cycle RMS, cursor RMS, duty cycle, phase, and delay. A waveform data-logging function can be used to save up to eight hours of triggered waveforms to a USB flash drive. Waveform limit testing lets the scopes automatically monitor signal changes and output pass/fail results.

The scopes provide USB connectivity, FFT capability, and a user interface that offers intuitive operation familiar to engineers.

Prices range from $520 for a two-channel, 25-MHz oscilloscope to $1520 for a two-channel, 150-MHz instrument.

—by Susan Nordyk

▷**Tektronix**, www.tek.com



The TBS1000 series gives users a choice of bandwidths, with sampling rates of 500M samples/sec for the 25- and 40-MHz scopes and 1G sample/sec for the 60-, 100-, and 150-MHz scopes.

TALKBACK

"High-voltage dc transmission lines are definitely the future for power-distribution systems ... [but] Edison's approach to proving ac more dangerous than dc was extremely unfortunate and wrongheaded. Death from either dc or ac is still death."

—Commenter rosekgiz, responding to the Power Management Design Center article "Has Thomas Edison ultimately won the dc vs ac power-transmission controversy against Tesla?" at www.edn.com/4404090. Add your own comment.

Self-contained Wi-Fi module eases IOT connectivity

Texas Instruments' SimpleLink Wi-Fi CC3000 module promises to simplify device connectivity on the Internet of Things (IOT).

The IOT enables devices to be wirelessly connected to the home network and to the cloud. "Headless" devices with no keypads or touchscreens, however, such as garage-door openers, home appliances, lights, thermostats, and treadmills, can be complicated to connect to a Wi-Fi network.

The self-contained SimpleLink Wi-Fi CC3000 module features SmartConfig technology, which is a TI-developed Wi-Fi configuration process that lets multiple in-home devices without displays connect to a Wi-Fi network via a smartphone or tablet in one step.

The module also supports service-discovery applications on phones, tablets, and PCs using Bonjour zero-configuration networking technology, letting consumers quickly identify and manage networked devices with greater ease.

The SimpleLink Wi-Fi CC3000 module is compatible with low-cost, low-memory microcontroller systems, such as TI's MSP430 family.

Production modules are slated to ship in the first quarter of this year through TI-authorized distributors for $9.99 (1000). The SmartConfig technology iOS app is available on the App Store; an Android version is expected this quarter.

—by Paul Buckley
▷**Texas Instruments**, www.ti.com

The self-contained SimpleLink Wi-Fi CC3000 features a TI-developed Wi-Fi configuration process that lets devices without displays connect to a Wi-Fi network via a smartphone or tablet in one step.

The connected car as a platform

When people think of the connected car, they think of a car that hooks to the cloud. The reality is that the car itself is a connected platform that enables multiple protocols to communicate and that connects to the cloud through the occupant's mobile cellular service and hardware.

Current models feature multiple communication systems that connect the engine, driver-assist, tire-pressure, airbag, safety, and camera/radar systems to the driver's display. There is also a network that connects the passenger area to the information system, along with entertainment control.

These systems are moving from wired platforms such as CAN, MOST, and FlexRay to standards such as Ethernet. New wired Ethernet solutions can support lightweight, unshielded cable capable of 100 Mbits/sec in full-duplex mode for connectivity.

Automakers such as BMW are pursuing such wired core systems to allow the car platform to be modeled on the data-center structure, with one in-platform interconnect system and a wireless or USB interface at the edge of the network. The wireless connections of choice are Wi-Fi and Bluetooth, both operating in the 2.4-GHz band.

This single-network configuration simplifies communications options by creating a single protocol for data transfer. Industry qualification to such global automotive standards as TS16949/ISO 9001, in-car EMC performance specs, and AEC-Q100 can be addressed in one pass. Automakers that adopt a single-interface system with unshielded cables can reduce system weight by as much as 30% and the cost of the connections by as much as 80% compared with previous approaches.

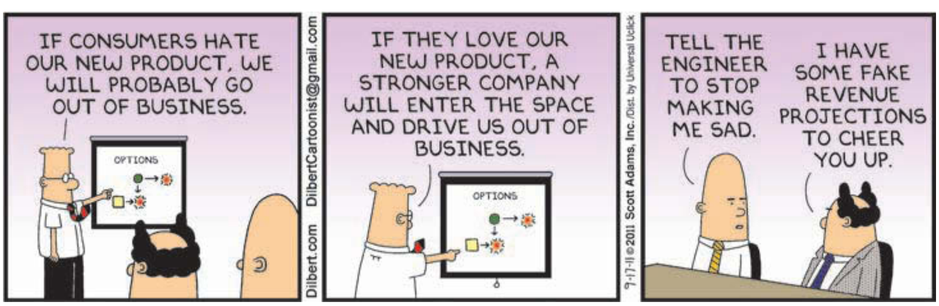
Automotive-grade (up to 85°C) communications solutions such as Broadcom Corp's BroadR-Reach address this market and are helping to fuel the work of the Automotive OPEN (one-pair Ethernet) Alliance special-interest group, which is promoting the switch to in-car Ethernet. The OPEN Alliance SIG has already registered more than 100 members.

The connected car is expected to push the automotive-semiconductor market to nearly $9 billion by 2018. The main roadblock has been the multiple noninterfacing data formats from separate subsystems that are tied to proprietary protocols. The rise in factory-installed networking connections reflects the integration of systems with sensor networks that are not accessible post-vehicle assembly. This factory-installed rate could soon approach 60%.

As the cost of connected-car systems comes down, they are becoming available in mass-market as well as luxury car models. The mass-market systems generally use dynamic database calls and temporary data storage, whereas the systems in luxury brands allow trend and knowledge data to be stored and analyzed in the vehicle as well as in the cloud.

—by Pallab Chatterjee
▷**Open Alliance SIG**, www.opensig.org

DILBERT By Scott Adams



LED-driver reference design has long lifetime, high efficiency

Power Integrations is offering a long-lifetime LED-driver reference design. DER-340 describes a wide-range (90 to 308V ac), high-power-factor LED-driver power supply that is suitable for high-bay, exterior, and street-lighting applications.

The LED driver detailed in DER-340 uses Power Integrations' LinkSwitch-PH power-conversion ICs, which combine single-stage power-factor correction and accurate constant-current output control. Single-stage LED-driver architectures typically yield up to 5% higher efficiency than two-stage designs, which combine losses from separate PFC and constant-current circuits. High-voltage aluminum-electrolytic bulk capacitors—the least reliable component in traditional lighting power-supply circuits—are not required in the single-stage approach, making 50,000-hour lifetimes attainable, according to Power Integrations.

In addition to providing an effective solution for standard lighting applications in benign environments, DER-340 copes with conditions of poor ventilation and high temperatures in industrial applications through the use of ceramic output capacitors and an accurate hysteretic thermal shutdown feature included in the LinkSwitch-PH IC.

The single-stage topology also reduces component count, letting developers use single-sided boards and smaller enclosures. DER-340 has an energy-efficient efficiency rating above 88% at 230V ac and more than 87% at 120V ac. Output-current tolerance is less than 5% across line, load, and temperature.

The LinkSwitch-PH ICs feature comprehensive integrated protection and reliability features, including output open-circuit/short-circuit protection with autorecovery; line input overvoltage shutdown, which extends voltage withstand during line faults; and autorecovering thermal shutdown with large hysteresis to protect both the components and the PCB.

DER-340 LED-driver power supplies meet all applicable international standards, including IEC 61000-4-5, IEC 61000-3-2 Class C, and EN55015 B.

A full schematic and reference design are available on Power Integrations' Web site. There is even a spec on how to design and create the inductor. **—by Steve Taranovich**

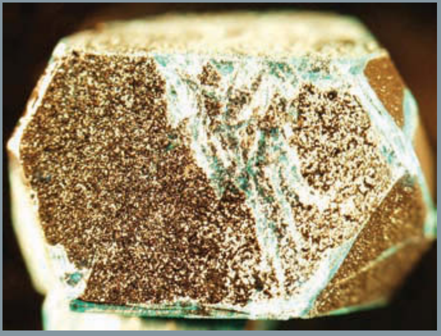
▷**Power Integrations**, www.powerint.com

The LED driver detailed in DER-340 uses Power Integrations' LinkSwitch-PH power-conversion ICs.

"Third state of magnetism" could advance storage, superconducting

A multidisciplinary team at the Massachusetts Institute of Technology claims to have demonstrated the existence of a long-theorized state of magnetism, called quantum spin liquid (QSL), that could have eventual application in computer memory storage and high-temperature superconductors. QSL is a solid crystal, but the fluctuating magnetic orientations of its individual particles resemble the constant motion of molecules within a liquid.

"We're showing that there is a third fundamental state for magnetism" in addition to ferromagnetism and anti-ferromagnetism, says MIT physics professor Young Lee, senior author of a paper on the work that appeared in the Dec 20, 2012, issue of *Nature* (http://bit.ly/VQazQw). There is no static order to the magnetic moments (orientations) within the material, "but there is a strong interaction between them, and due to quantum effects they don't lock in place," Lee adds.



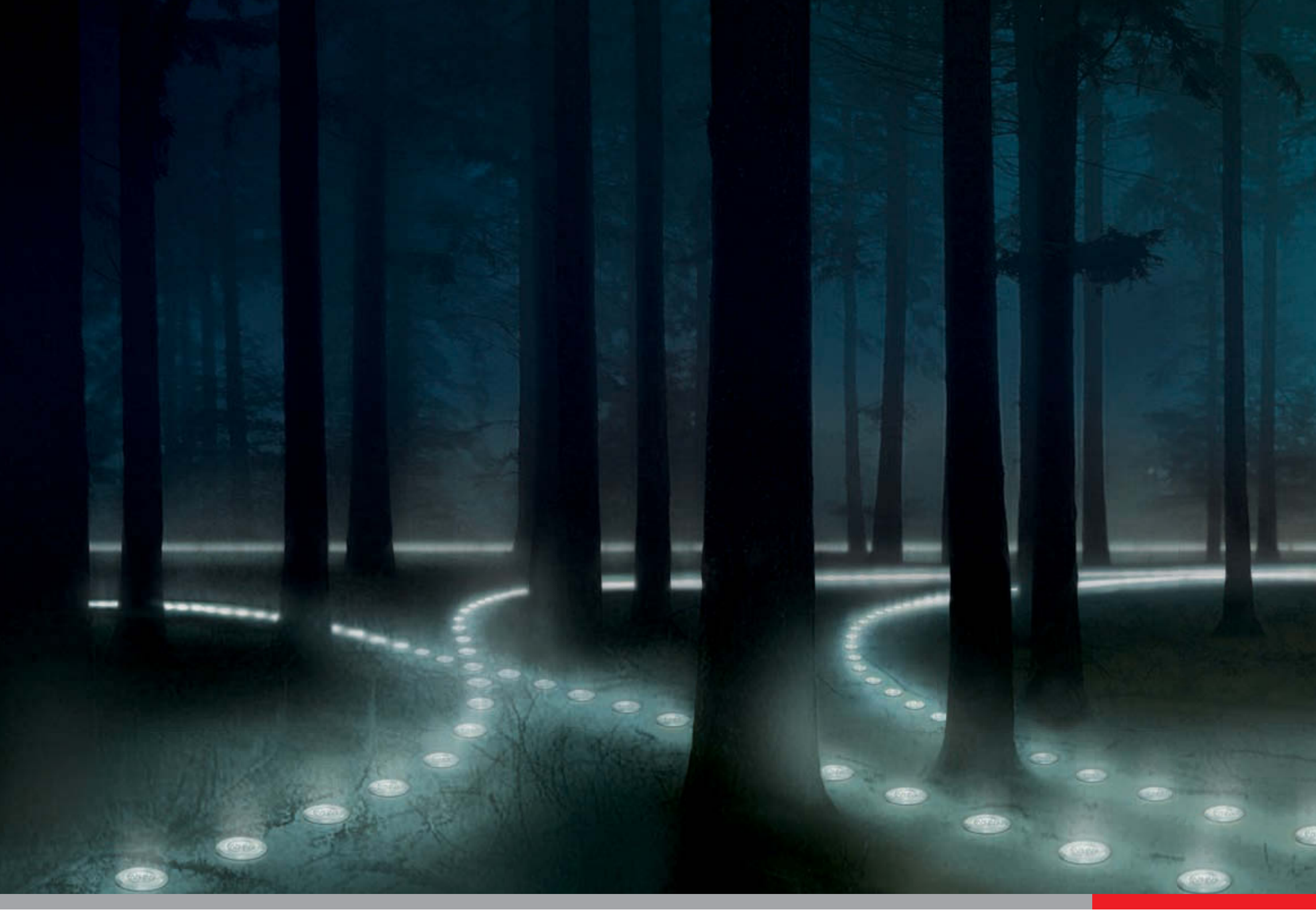
MIT physicists grew this pure crystal of herbertsmithite in their lab over a span of 10 months. The sample measures 7 mm long and weighs 0.2g (courtesy Tian-Heng Han).

The existence of QSLs has been theorized since 1987 but has been difficult to prove. MIT researchers spent 10 months growing a pure crystal of a suspected QSL material, herbertsmithite, and used a neutron spectrometer at the National Institute of Standards and Technology in Gaithersburg, MD, to analyze the material's structure through neutron scattering.

In their experiments on the crystal, the team found a state with fractionalized excitations; those excited states, called spinons, formed a continuum. "That's a fundamental theoretical prediction for spin liquids that we are seeing in a clear and detailed way for the first time" through the team's fundamental research, says Lee.

Practical results are a long ways off, but the work could lead to advances in data storage or communications, perhaps using long-range quantum entanglement.—by Diana Scheben

▶**MIT**, www.mit.edu



Battery-operated unit detects PIM in remote locations

Engineers at Anritsu have made the company's passive intermodulation (PIM) test analyzer truly portable, having shrunk the dimensions to one-quarter of the earlier tester's size and enabled battery operation of roughly 2.5 hours between charges. The changes allow testing for PIM in remote radio-head and indoor distributed-antenna systems.

The PIM Master MW82119A runs roughly 2.5 hours between battery recharges.

The PIM Master MW82119A tests at 40W and includes Anritsu's "distance to PIM" feature, which provides insight into where the PIM problem is, even if it is outside the antenna system. Power can be adjusted down to 0.3W to look for PIM on lower-power systems. There are six new models, covering the upper and lower 700-MHz bands, 850 MHz, 900 MHz, 1800 MHz, 1900 MHz, and 1900/2100 MHz.

The PIM Master includes standardized testing setups. A feature available as an option lets users stamp their tests with GPS information. The testers come with ac and automotive adapters; both recharge the battery.

Operating modes include PIM versus time measurement (a new mode), swept PIM measurement (mostly for factory testing), and the aforementioned distance-to-PIM measurement. With an optional USB power meter, the PIM analyzer can operate in power-meter mode. The PIM Master also has report-management capabilities, letting users overlay PIM plots to compare different lines; store the results; and create a unified test report that includes PIM, VSWR, distance to fault, and distance to PIM.

The handheld PIM analyzers are designed to withstand the same rugged conditions as the company's other portable products. Anritsu subjects the units to 50-hour burn-in and 2-hour thermal cycles.

Prices start at $22,995. Delivery is four to six weeks.

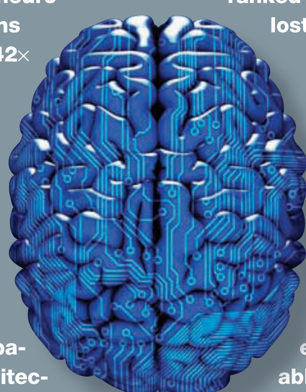
—by Janine Love

▷**Anritsu**, www.anritsu.com

The electronic brain gets closer

An IBM supercomputer has achieved a milestone in fulfilling the Defense Advanced Research Projects Agency's vision of developing electronic neuromorphic (brain-simulation) machine technology that scales to biological levels. At the Supercomputing 2012 conference, IBM announced it had simulated an unprecedented scale of 2.084 billion neurosynaptic cores containing 53×10^{10} neurons and 1.37×10^{14} synapses running only 1542× slower than real time.

DARPA's Systems of Neuromorphic Adaptive Plastic Scalable Electronics (SyNAPSE) program ultimately calls for building a cognitive computing architecture with 10^{10} neurons and 10^{14} synapses—a number inspired by the estimated number of synapses in the human brain. What IBM has achieved, using its Compass scalable simulator for the company's TrueNorth Cognitive Computing architecture, is not a biologically realistic simulation of the complete human brain but a simulation of "a novel modular, scalable, non-von Neumann, ultralow-power cognitive computing architecture at the scale of the DARPA SyNAPSE metric," according to the company.



The computing resources required for the latest simulation involved 1,572,864 processor cores and 1.5 PB of main memory. The simulation was powered by the Lawrence Livermore National Lab Blue Gene/Q Sequoia supercomputer. That machine currently is ranked the second fastest in the world, having lost the top spot to the Cray Titan.

Cognitive computing research promises systems that will be able to "learn through experiences, find correlations, create hypotheses, and remember and learn from the outcomes," according to IBM.

Dharmendra S Modha, a manager and lead researcher of the Cognitive Computing group at IBM Almaden Research Center, explains recent advances in the discipline in a short video viewable at www.edn.com/4402372. For details on the latest milestone, read the original IBM research report on Modha's Cognitive Computing blog at http://bit.ly/WvybzP.—by Rich Pell

▶**IBM**, www.IBM.com

BY BONNIE BAKER

What does "rail to rail" output operation really mean?

The advertisements for single-supply operational amplifiers often claim rail-to-rail output capability. What does this assertion really mean? Page one of a single-supply op amp's data sheet may call out "rail-to-rail input/output swing" in the title or bullets; read on, because if you are looking for a single-supply amplifier whose output can be driven all the way to one supply rail and/or the other, good luck. So, what should you know about an amplifier's performance that claims rail-to-rail output operation?

Two amplifier specifications will help you sort out this problem: output-voltage swing and open-loop voltage gain.

The output-voltage swing of an op amp defines how far you can drive the amplifier output toward the positive or negative supply rail. The output-voltage-swing high (V_{OH}) and output-voltage-swing low (V_{OL}) test conditions usually take the amplifier outside its linear region. The amplifier's open-loop-voltage-gain (A_{VOL}) specification primarily is the ratio of the closed-loop, output-voltage change to the input-offset-voltage change, but it also provides output-linearity hints in the test conditions.

The V_{OH} and V_{OL} specifications tell us how close the output pin comes to the power-supply rails. **Figure 1** shows a single-supply amplifier's output behavior. The output stage's transistors prevent the amplifier from reaching either rail.

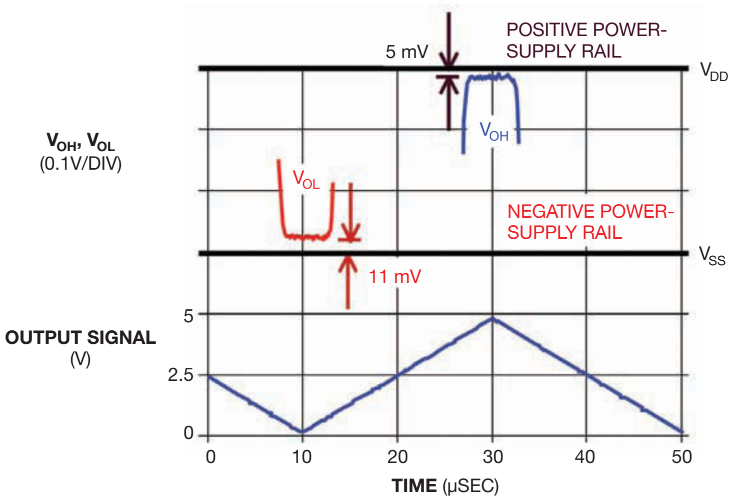


Figure 1 The output signal ramping from V_{SS} (GND) to the positive power supply (V_{DD}=5V) never reaches either rail. At ground, the amplifier stops at ~11 mV from the rail; at V_{DD}, the amplifier stops at ~5 mV from the rail.

As you examine these specifications with respect to their test conditions, you will find that the amplifier's output swing is dependent on the amount of current that the output stage is driving into the load. As you can see in **Table 1** (Amplifier A), viewable in the online version of this article at www.edn.com/4404550, the defined conditions of this specification have a significant influence on the amplifier's output performance. As the **table** shows, V_{OH} is the difference between V_{DD} (positive supply). V_{OL} is the difference between the minimum voltage out and V_{SS} (negative supply).

The key to comparing V_{OH} and V_{OL} from amplifier to amplifier is to determine the sink or source current. Smaller output currents provide better output-swing performance.

V_{OH} and V_{OL} tell us how close the amplifier drives to the rails but do not imply that the amplifier is linear so close to the supply voltage rails; the conditions of the A_{VOL} specification, by contrast, do. Measure A_{VOL} by comparing the amplifier's output swing in its linear region with the amplifier's input offset voltage. The dc open-loop gain is equal to the following **equation**:

$$A_{VOL}=20*\log(\Delta V_{OUT}/\Delta V_{OS}),$$

where ΔV_{OUT} is the dc change in output voltage and ΔV_{OS} is the dc change in input offset voltage.

Table 2 (Amplifier B), also at www.edn.com/4404550, shows an example of the A_{VOL} specifications and test conditions for a single-supply amplifier. In the condition column, note that the high and low output ranges of the amplifier are 5 mV from the power supplies. The A_{VOL} specification verifies that the amplifier is in its linear region.

If you are looking at a single-supply op amp that's claimed to offer rail-to-rail operation, make sure you look deeper before using the product in your application. Consider the V_{OH}, V_{OL}, and A_{VOL} specifications and conditions. Doing so will keep you from wasting your time and will ensure that you have the correct amplifier for your circuit. EDN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Noise-canceling headphones don't miss a beat

I recently wrote about my ongoing search for the perfect truly mobile audio-reproduction experience, and afterward one of you was kind enough to send me a set of NC-255 active-noise-reduction headphones. Manufactured by Hong Kong-based ODM Cobalt Industries and retailing for between $60 and $80, the headphones deliver decent audio at relatively low cost, but what made them particularly interesting to me was the effectiveness of the active noise reduction. I had to dig deeper.

Though the feature is intended for frequent fliers who want to attenuate cabin and engine noise, I tested the headphones' noise-reduction capability as I sat in a hotel room with my wife and two playing kids nearby, to see whether I could be blissfully unaware of my surroundings while listening to my tunes. Success! Even better, when my attention was (frequently) required, I didn't have to remove the headphones to listen; a very friendly "hear around you" button attenuated my music and amplified my surroundings. Life just keeps getting easier.

Noise cancellation has been around for years but continues to advance through better algorithms, processes, and methodologies. As mobile applications proliferate, however, power consumption is where the rubber hits the road. That's why I needed to look inside the headphones and see how the design could get 32 hours off a single AAA battery.

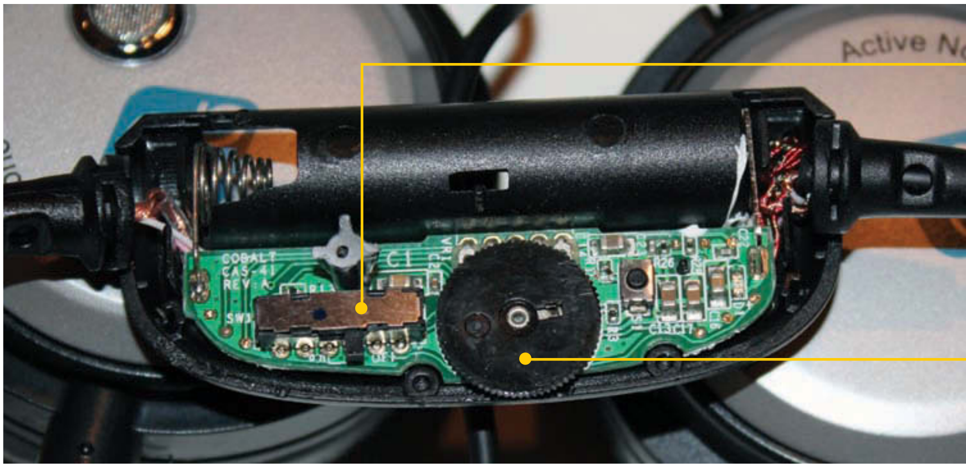
The NC-255 noise-cancellation controller's "hear around you" feature attenuates in-line audio and amplifies ambient sounds when necessary. The device achieves up to 25-dB noise reduction and runs off a single 1.5V AAA battery.

The NC-255 uses feed-forward active noise cancellation, which senses the noise on the outside of the headphone through this ambient-noise mic pickup. Feedback-based approaches, by contrast, accomplish noise sensing in the ear cavity.

On opening the controller, I found the AS3501 all-analog active-noise-cancellation IC from AMS.

We like digital noise reduction for its flexibility, but Oliver Jones, marketing manager for power management at AMS, says it's better to perform the filter-based phase adjustment and signal amplification in the analog domain to meet stringent audiophile requirements and minimize power consumption. I would agree, but of course the devil is in the implementation details.

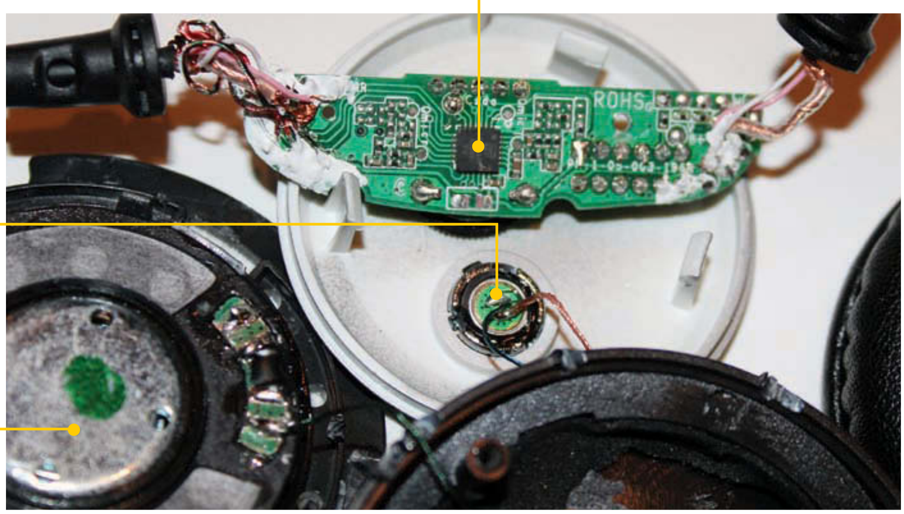
The AS3501 has proved itself, having been around since 2009, and now costs around $2 (1000). Eight more iterations have followed the introduction; the latest includes Bluetooth for a marginal price increase, to $2.15. AMS provides full design help, and the device is also in OEM brands such as Pinteo and Tivoli. Cobalt also manufactures the NC-255 on an ODM basis for brands such as AT&T, Beats, and Klipsch.



Active-noise-reduction on/off switch

Volume-control wheel

AMS' AS3501 speaker amplifier and active-noise-canceling IC features 0.6-μA quiescent current, true ground, a charge pump for microphones, 0.1% total harmonic distortion, >100-dB signal-to-noise ratio, I²C input, and one-time-programmable ROM.

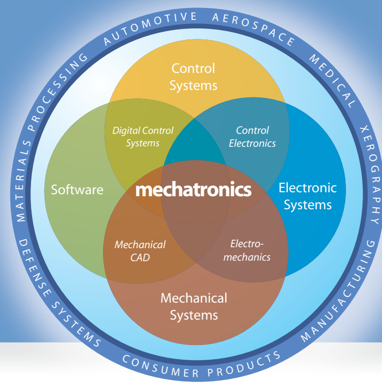


The deconstructed headphone offers this rear view of the mic pickup.

40-mm cobalt magnet speaker driver with 32Ω impedance

MECHATRONICS IN DESIGN

FRESH IDEAS ON INTEGRATING MECHANICAL SYSTEMS, ELECTRONICS, CONTROL SYSTEMS, AND SOFTWARE IN DESIGN



Forgotten practice can save US industry $500 billion a year

Tribology—the science of friction, lubrication, and wear—must be rediscovered.

By Kevin C Craig, PhD

US engineering advancement has been catalyzed over the decades by external threats: the Space Race threat from the Soviet Union in the 1960s; the economic threat from Japan's low-cost, high-quality manufacturing in the 1970s; the demographic threat from post-World War II engineering retirements in the 1980s; the global threat as US competitiveness declined in the 1990s; and now the environmental threat driving the need for global energy conservation and sustainability. In addition, the impending retirement of the Baby Boom generation challenges the engineering profession, as these workers will take with them a vast amount of knowledge and skill that must be replaced.

One critical area, essential in manufacturing and transportation, is tribology, officially defined in 1966 as the science and technology of interacting surfaces in relative motion. An undergraduate engineering student receives less than one hour of instruction in tribology during a four-year program, so this matter demands urgent attention.

Tribologists, through the development of air-bearing technology between 1960 and 1980, enabled the extremely fast, reliable, precise, and accurate operation of a computer hard-drive read/write head (approximately 0.05×0.04×0.01 in.) riding over the disk surface on a cushion of air at a height of 15 nm and an average speed of 53 mph. The challenge for tribologists today is to understand the potential modes for wear and surface damage in an endless variety of mechanical systems.

Whether the goal is to reduce parasitic friction or enhance friction in a design, the designer must employ a proper tribological approach—the right combination of geometry, materials, and lubrication—to ensure safety, performance, and energy-efficient operation. Estimates are that the correct application of tribology throughout US industry could save $500 billion annually.

Friction, inevitably accompanied by wear, accounts for most of the energy consumed in our society. The object of lubrication is to reduce friction, wear, and heating of machine parts, which move relative to each other. A lubricant is any substance that, when inserted between moving surfaces, accomplishes those purposes.

Several types of lubrication exist: *Hydrodynamic* refers to full-fluid-film lubrication, *hydrostatic* refers to lubricant introduced under pressure to create a full film, *elastohydrodynamic* refers to lubricant films between elastically deformable surfaces, *boundary* refers to a fluid film several molecular dimensions thick, and *solid* refers to solid lubricants used at high temperatures. Unlubricated surfaces have a friction coefficient of about 1.0 with heavy wear; for boundary and thin-film lubrication, the value is about 0.01 with slight wear; and for thick-film lubrication, the value is about 0.001 with no wear.

The most common fluid-film bearing is the journal bearing, in which a sleeve of bearing material is wrapped partially or completely around a rotating shaft to support a radial load. **Figure 1** shows a plot of the coefficient of friction versus Hersey number (μN/P, where μ is the absolute viscosity in centipoise, N is the shaft speed in rpm, and P is the average pressure in psi) for a journal bearing under test conditions, and is a good measure of the state of health of the bearing.

There are other areas of science and technology that, like tribology, are threatened. Once these skills and knowledge are lost, getting them back will be nearly impossible. EDN

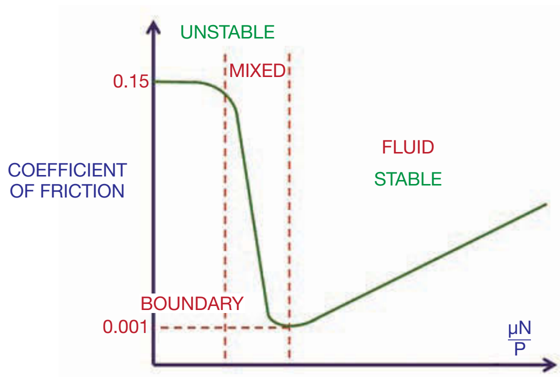


Figure 1 This plot of the coefficient of friction versus Hersey number for a journal bearing under test is a good measure of the health of the bearing.

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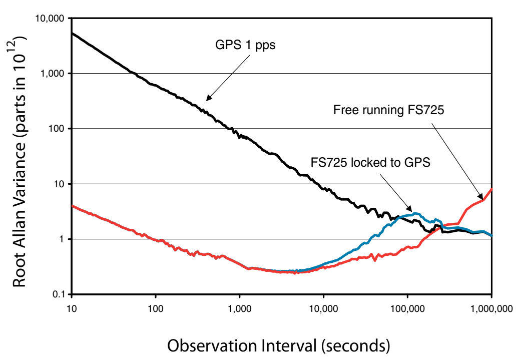

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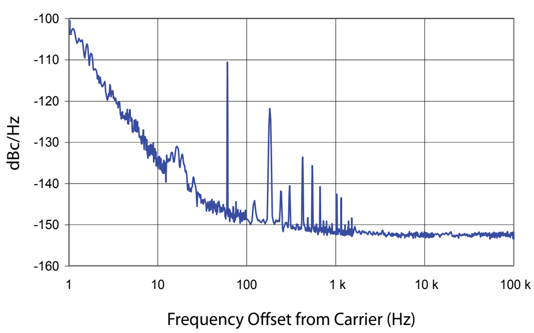

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DETECTING AND DISTINGUISHING CARDIAC-PACING ARTIFACTS

BURIED IN NOISE AND LARGER CARDIAC SIGNALS, THE ARTIFACTS OF A PACEMAKER ARE DIFFICULT TO SPOT. THE METHODOLOGY PRESENTED HERE CAN HELP DIAGNOSTICIANS READ BETWEEN THE LINES OF AN ECG STRIP.

JOHN KRUSE AND CATHERINE REDMOND • ANALOG DEVICES INC

When a heart patient with an implanted pacemaker undergoes electrocardiogram testing, the cardiologist must be able to detect the presence and effects of the pacemaker (see **sidebar**, "When the heart's electrical subsystem malfunctions," available with the online version of this article at www.edn.com/4404758). A simple implanted pacer's activity is generally not perceptible on a normal ECG trace, because the very fast pulses—with typical widths of hundreds of microseconds—get filtered due to low-bandwidth display resolution (monitor/diagnostic 40-/150-Hz bandwidths). The pacer's signal, however, can be inferred through the changed morphology of the ECG trace, which is representative of the heart's own electrical activity as recorded at the skin surface via ECG leads.

IMAGE: ISTOCK

It is important to be able to detect and identify pacing artifacts because they indicate the presence of the pacemaker and help in evaluating its interaction with the heart. But the artifacts' small amplitude, narrow width, and varying waveshape make them difficult to detect, especially in the presence of electrical noise that can be many times their amplitude. At the same time, pacing therapy has become extremely advanced, with dozens of pacing modes available for single- to three-chamber pacing. Complicating the detection of pacing artifacts, pacemakers produce lead-integrity pulses, minute-ventilation (MV) pulses, telemetry signals, and other signals that can be incorrectly identified as pacing artifacts.

The use of real-time pacemaker telemetry has made the display of pacing artifacts on an ECG strip less important than it used to be. An individual skilled in pacing therapies can look at the strip and sometimes infer the type of pacing therapy being administered to the patient and determine whether the pacemaker is working properly.

In addition, all pertinent medical standards require the display of pacing artifacts, though they vary somewhat in their specific requirements for the height and width of the captured pacer signal. The applicable standards include Association for the Advancement of Medical Instrumentation (AAMI) specifications EC11:1991/(R)2001/(R)2007 and EC13:2002/(R)2007, as well as International Electrotechnical Commission specifications IEC 60601-1 ed. 3.0b:2005, IEC 60601-2-25 ed. 1.0b, IEC 60601-2-27 ed. 2.0:2005, and IEC 60601-2-51 ed. 1.0:2005.

AT A GLANCE

- A simple implanted pacer's activity is generally not perceptible on a normal ECG trace, because the very fast pulses get filtered out. Individuals skilled in pacing therapies, however, can examine the ECG trace to confirm the presence of a pacemaker and evaluate its interaction with the heart.
- Artifacts from implanted pacemakers can vary from 2 to 700 mV, with durations between 0.1 and 2 msec and rise times between 15 and 100 µsec. The presence of electrical noise that can be many times their amplitude makes the pacing artifacts difficult to detect.
- A major noise source is the H-field telemetry scheme used by most implantable heart devices.
- The ADAS1000 ECG analog front end embeds an algorithm that can help distinguish pacing artifacts and display them on the ECG strip chart.

HOW PACEMAKERS PACE

Implantable pacemakers (**Figure 1**) are typically lightweight and compact. They contain the circuitry necessary to monitor the heart's electrical activity through implanted leads and to stimulate the heart muscle as necessary to ensure a regular heartbeat. Pacemakers must be low-power devices, as they operate with a small battery that typically has a 10-year lifespan. The National Academy of Engineering estimated in 2010 that more than 400,000 pacemakers are implanted in patients every year (**Reference 1**).

In unipolar pacing, the pacing leads consist of an electrode at the tip of a single pacing lead and the metal wall of the pacemaker housing itself. The pacing artifacts caused by this mode of pacing can be several hundred millivolts at the skin surface, with a width of up to 2 msec. Unipolar pacing is no longer commonly used, however.

In bipolar pacing, which today accounts for the bulk of pacing artifacts created, the heart is paced from the electrode at the tip of the pacing lead. The return electrode is a ring electrode located very close to the tip electrode.

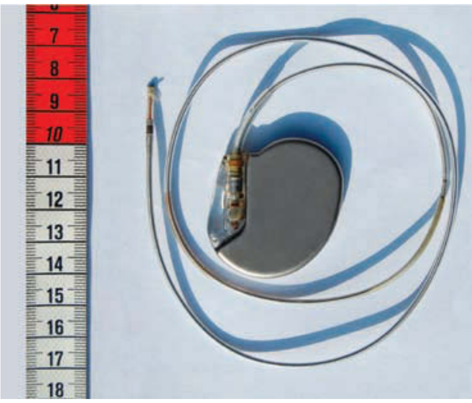

Figure 1 Pacemakers must be light, compact, low-power devices (**Reference 2**).

The artifacts that this type of lead produces are much smaller than those produced by unipolar pacing; pulses on the skin surface can be as small as a few hundred microvolts high and 25 µsec wide, with average artifacts measuring 1 mV high and 500 µsec wide. The amplitude of the artifact can be much smaller when the detection vector does not line up directly with the pacing lead vector.

Many pacemakers can be programmed for pulse widths as short as 25 µsec, but the short-pulse-width settings are typically used only in pacemaker threshold tests performed in an electrophysiology laboratory. Setting the lower limit to 100 µsec eliminates the problem of falsely detecting MV and lead-integrity (LV lead) pulses as valid pacing artifacts. These subthreshold pulses are usually programmed to be between 10 and 50 µsec.

Various types of pacemakers are available for pacing specific chambers of the heart. Single-chamber pacing delivers pacing therapy to either the right atrium or the right ventricle. Such a pacer can be either unipolar or bipolar. Dual-chamber pacing delivers pacing therapy to both the right atrium and the right ventricle. Biventricular pacing delivers pacing therapy to both the right ventricle and the left ventricle; in addition, the heart is usually paced in the right atrium.

The biventricular pacing mode can be difficult to display properly, for two main reasons. First, the two ventricle paces may occur at the same time, appearing as a single pulse at the skin surface. Second, the left-ventricle lead placement is generally not on the same vector as the right-ventricle lead and may actually be orthogonal to it. Usually, the right atrium is best displayed in lead aVF—one of the augmented limb leads—and the right ventricle is best displayed in lead II. Most ECG systems do not employ three simultaneous lead-detection circuits or algorithms, making the left ventricle the toughest lead to pick up. Thus, it is sometimes best detected in one of the V leads.

ARTIFACT WAVEFORMS

Most pacing pulses have very fast rising edges. The rise time measured at the pacemaker output is generally about 100 nsec. When measured at the skin surface, the rise time will be slightly slower because of the inductance and capacitance of the pacing lead. Most pacing artifacts at the skin surface are on the order of 10 μsec or less. As complex devices with built-in protection, pacemakers can produce high-speed glitches that do not affect the heart but do affect pacemaker-detection circuits.

PACING ARTIFACTS' SMALL AMPLITUDE, NARROW WIDTH, AND VARYING WAVESHAPES MAKE THEM DIFFICULT TO DETECT.

Figure 2 shows an example of an ideal pacing artifact. The positive pulse has a fast rising edge. After the pulse reaches its maximum amplitude, a capacitive droop follows, and then the trailing edge occurs. The artifact next changes polarity for the recharge portion of the pacing pulse. The recharge pulse is required so that the heart tissue is left with a net-zero charge; with a monophasic pulse, ions would build up around the electrodes, creating a dc charge that could lead to necropsy of the heart tissue.

Introducing cardiac-resynchronization devices adds another degree of complication in detecting and displaying pacing artifacts. These devices pace the patient in the right atrium and both ventricles. The pulses in the two ventricles can fall close together, overlap, or occur at exactly the same time; the left ventricle can even be paced before the right ventricle. Currently, most devices pace both ventricles at the same time, but studies have shown that adjusting the timing will benefit some patients by yielding a higher cardiac output.

Detecting and displaying both pulses separately is not always possible, and many times the pulses will appear as a single pulse on the ECG electrodes. If both pulses were to occur at the same time with the leads oriented in opposite directions, the pulses could cancel each

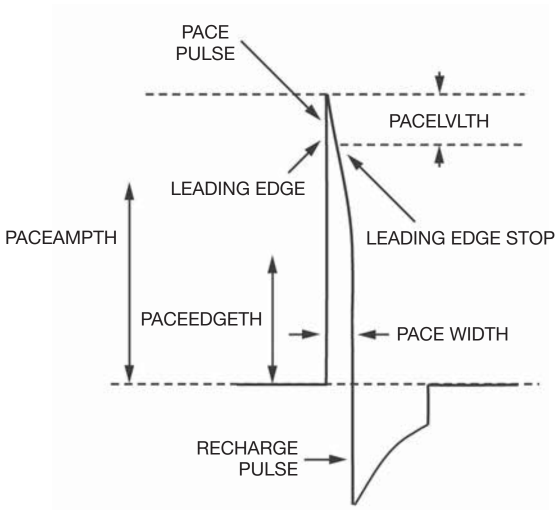

Figure 2 In this example of an ideal pacing artifact, the positive pulse has a fast rising edge. After the pulse reaches its maximum amplitude, a capacitive droop follows, and then the trailing edge occurs. The artifact then changes polarity for the recharge portion of the pacing pulse.

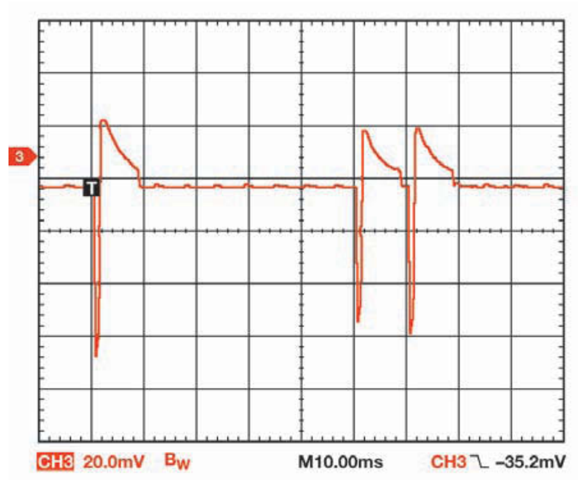

Figure 3 Scope traces are shown for a cardiac-resynchronization device pacing in a saline tank—a standard test environment for pacemaker validation.

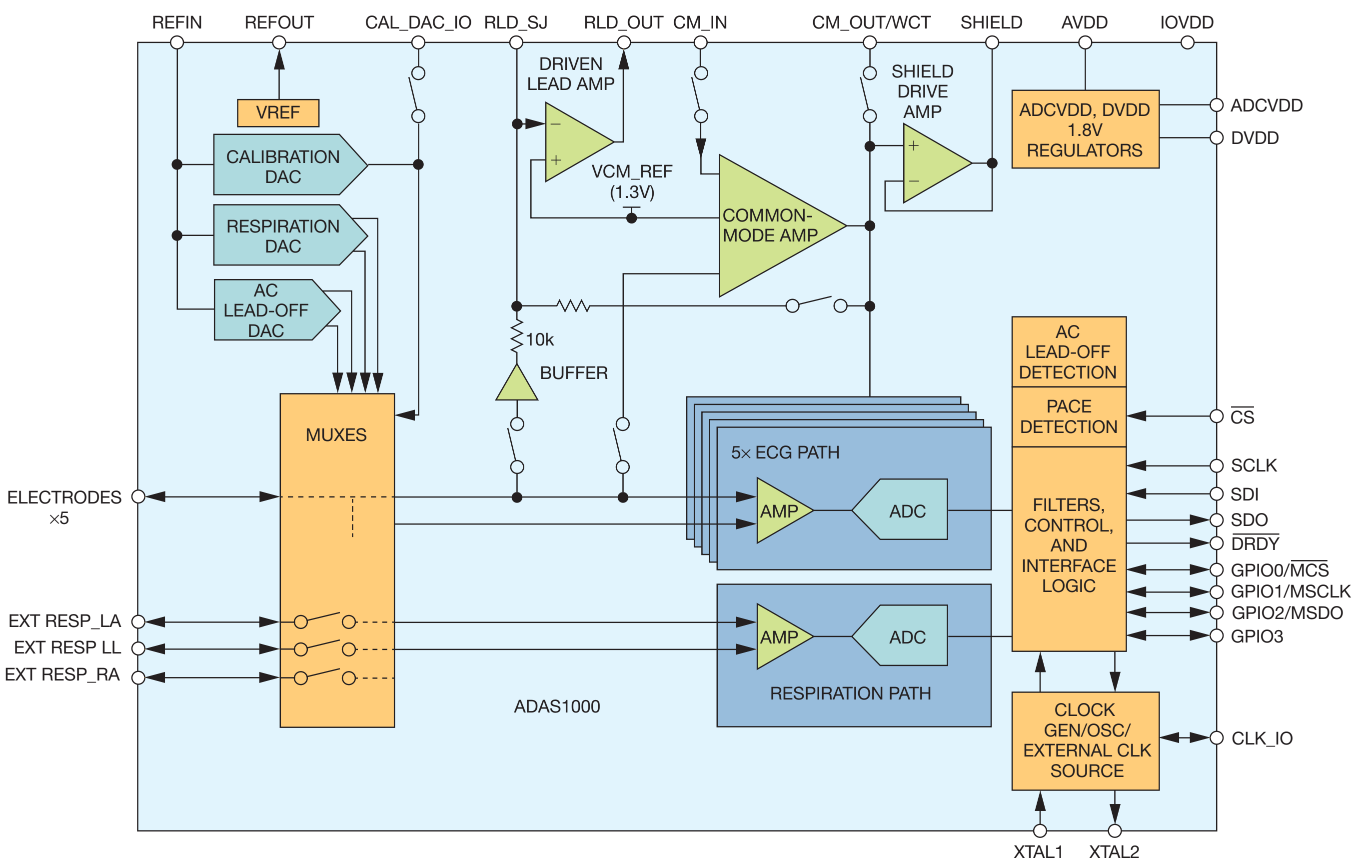

Figure 4 The block diagram shows the ADAS1000 analog front end.

other out on the skin surface. The probability of such an occurrence is remote, but one can envision the appearance on the skin surface of two ventricle-pacing artifacts with opposite polarities. If the two pulses were offset by a small time interval, the resulting pulse shape might be very complex.

Figure 3 shows scope traces of a cardiac-resynchronization device pacing in a saline tank. This is a standard test environment for pacemaker validation, designed to mimic the conductivity of the human body. The proximity of the scope probes to the pacing leads causes the amplitudes to be much larger than what would be expected on the skin surface, however, and the low impedance that the saline solution presents to the ECG electrodes results in much less noise than would normally be seen in a skin-surface measurement.

The first, second, and third pulses shown in the **figure** (l to r) are the atrial, right-ventricle, and left-ventricle pulses, respectively. The leads were placed in the saline tank with vectors optimized to see the pulses clearly. The negative-going pulse is the pace; the positive-going pulse is the recharge. The amplitude of the atrial pulse is slightly larger than the two other pulse amplitudes because the lead was in a slightly better vector than the ventricle leads; in actuality, all three pacing outputs in the resynchronization device were programmed to have the same amplitude and width. With real patients, the amplitudes and widths are often different for each pacemaker lead.

ARTIFACT DETECTION

It is impossible to detect all pacing artifacts and reject all possible noise sources in a cost-effective manner. Among the challenges are the number of chambers that the pace detection must monitor, the interference signals encountered, and the wide variety of pacemakers in use. Solutions for detecting artifacts may range from hardware implementations to digital algorithms.

The pacing leads for cardiac-resynchronization devices will not all have the same vector. The right-atrium lead usually aligns with lead II, but it can sometimes point straight out of the chest, so a Vx (precordial lead) vector may be needed to see it. The right-ventricle lead is usually placed at the apex of the right ventricle, so it usually aligns well with lead II. The left-ventricle pacing lead, threaded through the coronary sinus, is actually on the outside of the left ventricle. This lead usually aligns with lead II but may have a V-axis orientation.

The pacing leads of implantable defibrillators and resynchronization devices are sometimes placed in areas of the heart that have not had an infarction. Placing them around infarcts is the main reason that this system uses three vectors and requires a high-performance pacing-artifact detection function.

A major noise source is the H-field telemetry scheme used in most implantable heart devices. Other sources of noise are transthoracic-impedance measurements for respiration, electric cautery, and conducted noise from other medical devices connected to the patient.

Complicating the problem of

acquiring pacing artifacts, each pacemaker manufacturer uses a different telemetry scheme. In some cases, a single manufacturer may use different telemetry systems for different implantable-device models. Many implantable devices can communicate using both H-field telemetry and either ISM- or Medical Implant Communication Service (MICS)-band telemetry. The variability of H-field telemetry from one model to the next makes filter design difficult. ECG devices have to be Class CF—the most stringent classification—as there is direct conductive contact with the heart, whereas other medical devices may be built to less stringent Class B or BF requirements, and their higher leakage currents may interfere with the performance of ECG-acquisition devices.

ARTIFACT-DETECTING AFE

The ADAS1000 (**Figure 4**) is a five-channel analog front end designed to address some of the challenges facing designers of low-power, low-noise, high-performance, tethered or portable ECG systems. The AFE, designed for both monitor- and diagnostic-quality ECG measurements, comprises five electrode inputs and a dedicated right-leg-drive (RLD) output reference electrode. In addition to supporting the essential ECG signal-monitoring elements, the AFE enables such functions as respiration (thoracic impedance) measurement, lead/electrode connection status, internal calibration, and capabilities for pacing-artifact detection.

One ADAS1000 supports five electrode inputs, facilitating a traditional, six-lead ECG measurement. By cascading a companion ADAS1000-2 device, the system can be scaled up to a true 12-lead measurement; by cascading three or more devices, the system can be scaled to measurements with 15 leads and beyond.

DETECTION ALGORITHM

The device's front end includes a digital pacemaker artifact-detection algorithm that detects pacing artifacts with widths ranging from 100 μsec to 2 msec and amplitudes ranging from 400 μV to 1000 mV, to align with AAMI and IEC standards. **Figure 5** is a flow diagram of the algorithm.

The pace-detection algorithm runs three instances of a digital algorithm on three of four possible leads (I, II, III, or aVF). It runs on the high-frequency ECG data, in parallel with the internal decimation and filtering, and returns a flag that indicates pacing was detected on one or more of the leads, providing the measured height and width of the detected signal. For

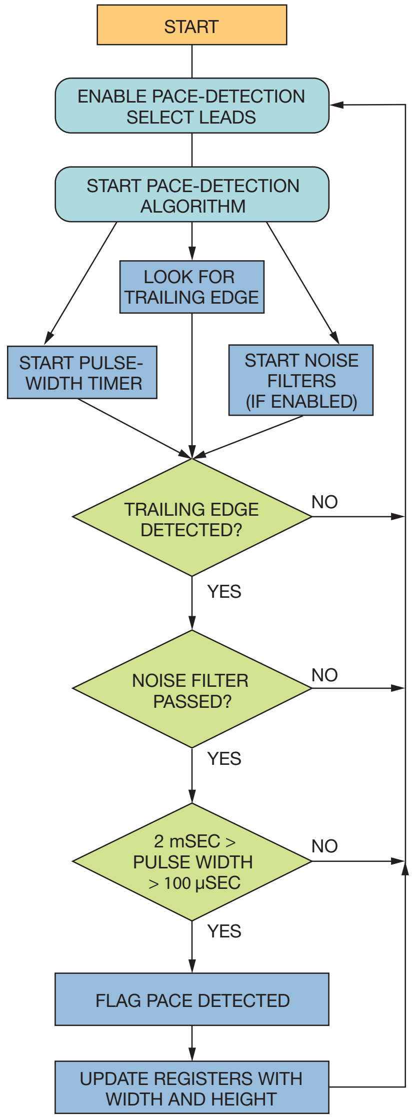

Figure 5 The flowchart shows the digital-pacemaker decision process for the artifact-detection algorithm, which detects pacing artifacts with widths that range from 100 μsec to 2 msec and amplitudes that range from 400 μV to 1000 mV.

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users who wish to run their own digital pace algorithm, the ADAS1000 supplies a high-speed pace interface that provides the ECG data at a 128-kHz data rate; the filtered and decimated ECG data remains unchanged on the standard interface.

A minute-ventilation filter is built into the ADAS1000 algorithm. MV pulses, which are conducted from the ring of a bipolar lead to the housing of the pacemaker, detect respiration rates to control the pacing rate. They're always less than 100 μsec wide, varying from about 15 to 100 μsec.

The simultaneous three-vector pacing-artifact system can detect pacing artifacts in noisy environments. Each of the three instances of the pace algorithm can be programmed to detect pace signals on different leads (I, II, III, or aVF). Programmable threshold levels tailor the algorithm to detect the range of pulse widths and heights presented, with internal digital filters designed to reject heartbeat, noise, and MV pulses. When a pace has been validated in an individual instance of the pace signal, the device outputs a flag so that the user can mark or identify the pace signal in the ECG capture strip.

The choice of sample rate for the pacing-artifact algorithm is significant because it cannot be exactly the same frequency as those used for the H-field telemetry carrier by the three pacing-systems companies (Boston Scientific, Medtronic, and St Jude). All three vendors use different frequencies, and each has many different telemetry systems. Analog Devices believes that the ADAS1000's sampling frequency does not line up with that of any of the major telemetry systems. **EDN**

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AUTHORS' BIOGRAPHIES

John Kruse is a field applications engineer for Analog Devices in Minneapolis. He joined ADI in 2005 and specializes in medical applications. He has authored many articles and patents; several of the patents cover pacing-artifact acquisition. Kruse graduated with a bachelor of science degree in electronics engineering from the University of Minnesota in 1980. In 1997, he received a master of science degree in electronics engineering from the University of St Thomas (St Paul, MN), where he currently is an adjunct professor.

Catherine Redmond is an applications engineer at Analog Devices in Limerick, Ireland. Since joining ADI in 2005, she has gained industrial-market expertise by supporting precision DACs as applied in automatic test equipment. Redmond currently focuses on precision ADC products. She graduated from Cork Institute of Technology in Ireland with a bachelor's degree in electronics engineering.

SIGNAL-INTEGRITY ISSUES ON THE RISE

JANINE LOVE • EDITOR IN CHIEF, *TEST & MEASUREMENT WORLD*

IMAGE: SHUTTERSTOCK

OUR VIRTUAL PANEL SHARES **EYE-OPENING** ADVICE FOR ANTICIPATING, DETECTING, AND MITIGATING SI PROBLEMS IN FASTER, INCREASINGLY COMPLEX DESIGNS.

Electronics design trends that ratchet up design complexity and speed, such as the use of multiple high-speed buses, bring new signal-integrity challenges. With that in mind, *EDN* assembled a virtual panel of engineers working in signal integrity to examine the current impairments, assess how well the available test equipment is measuring up, and determine what we can do both short- and long-term to improve signal integrity. Admittedly, there are many things that can affect signal integrity (**Reference 1**); in this discussion, we focus primarily on crosstalk and EMI.

WHAT'S THE PROBLEM?

Many a trained eye is focused on the effects of multiple high-speed buses on signal integrity and how to avoid the related problems. Chris Loberg, senior technical marketing manager at Tektronix Inc, and Tim Caffee, vice president for design validation and test at Asset InterTech Inc, agree that shrinking operating margins on high-speed buses are contributing to the challenges.

"The design trend is faster serial speeds, above 10 Gbits/sec, with no new cost-effective architecture for improving signal-path accommodation of issues like EMI and crosstalk," Loberg observes. "So, signaling accommodations like equalization must be made to minimize EMI and crosstalk effects, enabling the receiver to accurately determine the serial-bus logic transition."

Loberg notes that interval times—the time between a transition to one or zero—are shrinking; as a result, in a traditional eye diagram used to evaluate transitions, EMI and crosstalk are "closing" the eye. Engineers can no longer effectively evaluate signal integrity, as crossing points and timing-integrity evaluations become much more challenging.

Caffee notes that with each successive generation of high-speed bus, operating margins are gradually shrinking as signal frequencies increase, enabling effects such as jitter, intersymbol interference (ISI), and crosstalk to "create havoc" on the signal integrity of high-speed SerDes and memory channels. Each new step to a higher speed and signaling frequency makes the bus more susceptible to distortions and anomalies that can effectively disrupt traffic and stall system throughput.

The eye diagram in **Figure 1** illustrates this point, showing the effects of increasing signal frequencies on three generations of a hypothetical high-speed bus and the resultant, decreasing operating margins on the bus. As frequencies increase, even the slightest distortion can disrupt signaling throughput.

Alan Blankman, product manager for signal-integrity products at Teledyne LeCroy, agrees that higher bit rates (>25 Gbits/sec) and "parallelized serial" standards such as PCI Express (PCIe), 40/100GBase-R, and InfiniBand are contributing to signal-integrity issues. "Faster bit rates require faster edges with higher-frequency content, which results in bigger reflections due to impedance mismatches at connectors, vias, packages, etc.; higher levels of loss; and higher levels of crosstalk and EMI, due to increased coupling to neighboring traces," Blankman says.

Shamree Howard, signal-integrity program manager at Agilent Technologies, adds that faster speeds create issues for accurate data capture, requiring precise triggering. She says jitter measurements are the key to characterizing high-speed digital links, noting, "The measurement of jitter—even if the user is provided a one-button interface—is a sophisticated affair, taking into account clock recovery and knowledge of phase-locked loops, jitter decomposition techniques and assumptions for them, crosstalk and its effects, and waveform statistics that require different approaches" (**Reference 2**). Howard adds that the Agilent U4154A 4-Gbit/sec AXIe logic-analyzer module can make reliable measurements on eye openings as small as 100 psec × 100 mV (**Figure 2**).

Howard Johnson of Signal Consulting Inc concurs that circuits at very high speeds are notoriously difficult to probe. "Even in cases when a probe exists that can do the job, you often cannot place the probe at the point in a circuit that you wish to observe," says Johnson. He suggests that the answer is to use cosimulation, or the process of simultaneously developing both a physical circuit and a software simulation of it.

AT A GLANCE

- Each new step to a higher speed and signaling frequency makes the bus more susceptible to distortions and anomalies that can disrupt traffic and stall system throughput. "Parallelized serial" standards are contributing to signal-integrity issues. Circuits at very high speeds are notoriously difficult to probe.
- One way forward is to improve the signal path itself with an optical backplane; another way to improve signal integrity is to trick the signal using equalization approaches to minimize crosstalk.
- Many designers are managing crosstalk and EMI through better design practices around the signal path.
- Most engineers working on signal-integrity issues agree that simulation is becoming mandatory for high-speed system design.

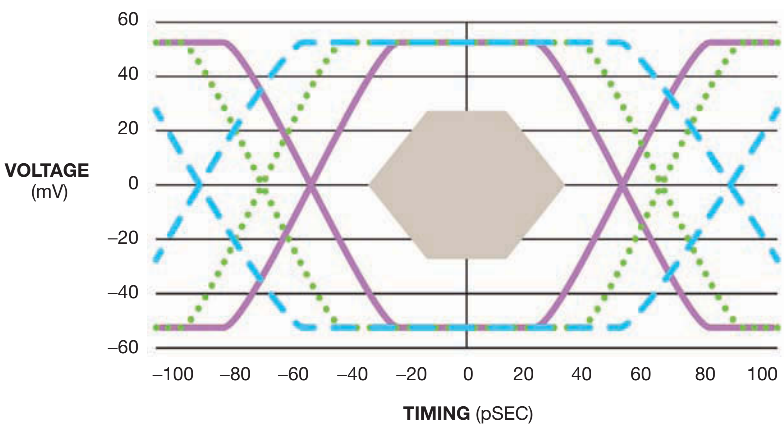

Figure 1 Moving from 6 (broken line) to 8 (dotted line) and, eventually, 10 Gbits/sec (solid line) closes the eye around the operational sweet spot at the center of the diagram (courtesy Asset InterTech).

DESPITE NEW OSCILLOSCOPE TECHNIQUES, THERE IS NO AUTOMATED WAY TO IDENTIFY CROSSTALK UNAMBIGUOUSLY.

The problem, observes Ransom Stephens of Ransom's Notes, is that, despite new oscilloscope techniques from leading manufacturers, there is no automated way to identify crosstalk unambiguously. The latest test products offer ways to estimate the effect of crosstalk on the bit error rate (BER), but they are all process-of-elimination approaches.

"Avoiding crosstalk is simple in principle but sometimes impossible in practice," Stephens acknowledges. Because crosstalk is caused by jolts of radiation when an aggressor signal makes a logic transition, increasing the rise/fall times will reduce crosstalk. Because it's interference, increasing trace separation has a big effect, too.

"I think that careful differential design is your best bet, though," Stephens offers. "If you can get the differential skew really small and get the two traces nearly on top of each other, then the cancellation from differential

signaling has a fighting chance."

HOW DO WE IMPROVE SI?

According to Tektronix's Loberg, there are several ways forward. First, change and improve the signal path itself. One way to do that is with an optical backplane; this is happening, but not in the mainstream (think Thunderbolt). Another way to improve signal integrity is to trick the signal using equalization approaches to minimize crosstalk; for instance, you could hard-code the chip or compile FPGA code to equalize the signal. In addition, many designers are managing crosstalk and EMI through better design practices around the signal path.

Asset InterTech's Caffee proposes that engineers validate signal integrity on the bus during each of the major phases of a system's life cycle, from design to field operation, though he recognizes that this is a challenging approach and thus not a popular one. If detected during prototype-board bring-up, signal-integrity problems could trigger changes in the design; if detected during manufacturing, problems could result in alterations to the production process. If problems are detected in the field as a result of troubleshooting poorly performing systems, design changes, manufacturing-process changes, or both should be made for the next product generation to reduce returns and warranty claims.

Figure 3 The Anritsu MP1800A 32G synchronized multi-BERTS and MP1825B 28.1G four-tap emphasis aim to assist signal-integrity analysis by keeping the eye open.

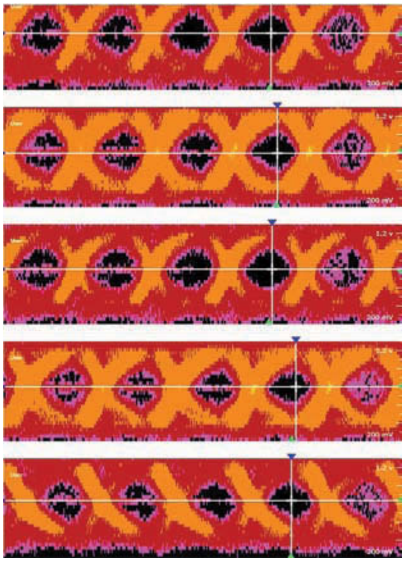

Figure 2 The Agilent U4154A logic analyzer uses its eye-scan capability to place the sampling point automatically in both time and voltage within the eye, making measurements on eye openings as small as 100 psec × 100 mV.

Hiroshi Goto, business development manager at Anritsu Co, suggests preemphasis as an effective transmission technique for maintaining the eye opening. With transmission speeds increasing to 20 Gbits/sec and faster, Goto proposes a three- or four-tap emphasis signal in order to increase the number of bits to be emphasized.

It's a complex job to check and set the combination of emphasis rates for each tap, however, making it difficult to find the ideal emphasis signal without quantitative guidelines.

The Anritsu-developed MP1825B four-tap emphasis and transmission-analysis software, working with the MP1800A signal-quality analyzer BER test set (BERTS), finds "the ideal emphasis settings based upon the reverse characteristics" of the device under test (DUT), says Goto (**Figure 3**). "This raises the height of the eye and keeps the eye open, allowing better quantitative signal-integrity analysis in the shortest amount of time."

SIMULATION AND VALIDATION

Most agree that simulation is becoming mandatory for high-speed system design. Agilent's Howard says the company's Advanced Design System (ADS) is the leading EDA software in use for high-speed digital applications.

Teledyne LeCroy's Blankman adds that to detect and mitigate crosstalk issues, designers must be able to predict near- and far-end crosstalk by running simulations, and to validate the models used in the simulations by taking measurements (**Figure 4**). To validate crosstalk models, designers need multidifferential-lane S-parameter measurements (eight-port for aggressor-victim models, 12-port for aggressor-victim-aggressor models, or even higher port counts).

Measuring crosstalk requires vertical noise measurements taken by real-time oscilloscopes that can extract the crosstalk from the serial data signal. Those measurements should estimate eye closure as a function of BER, as jitter measurements do. Jitter measurements are also important, of course. Measuring both jitter and noise yields a more complete picture of crosstalk than jitter measurements alone.

TOOLBOX

Test-equipment vendors are working to evolve their tools to characterize jitter and improve signal-integrity analysis, so the optimal toolbox for signal-integrity engineers may not yet be available. Signal Consulting's Johnson predicts that "the next trend will involve a blend of specialized equipment and test software designed to characterize a power system and inject specific test current waveforms into that power system." Stephens, of Ransom's Notes, suggests that we be on the lookout for more crosstalk-equalization techniques.

So, what's out there now?

• **Scopes.** Here is where high-bandwidth oscilloscopes can really prove their worth. Teledyne LeCroy's Blankman notes that nonreturn-to-zero (NRZ) serial data patterns can have rise times less than 30 psec. He points

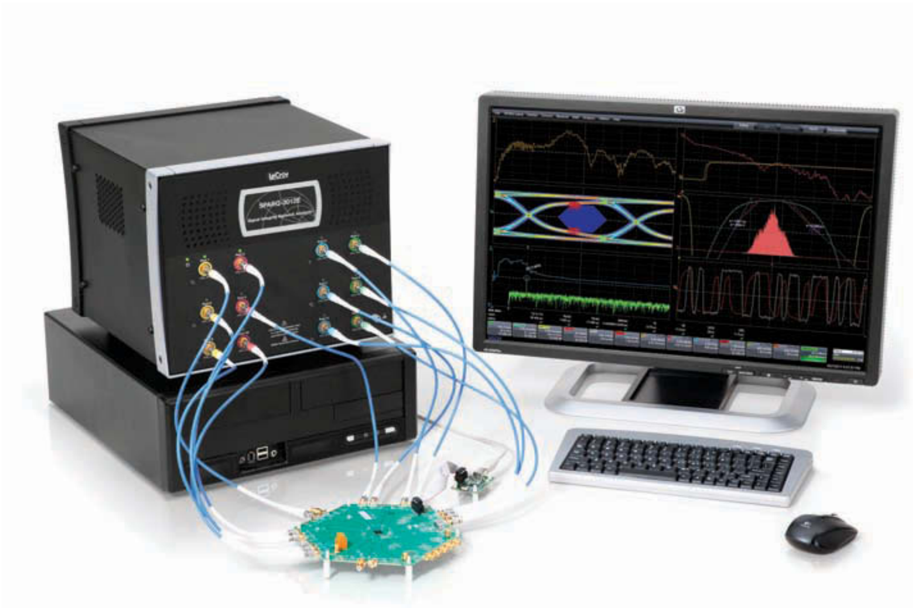

Figure 4 The SPARQ signal-integrity network analyzers from Teledyne LeCroy connect directly to the DUT and PC-based software through a single USB connection for quick, multiport S-parameter measurements.

out that receiver testing of PCIe Gen3 systems requires a scope with a 13-GHz bandwidth, whereas transmitter testing needs a 20-GHz scope.

"Emerging multilane designs like InfiniBand and 40/100GBase-R have even more-demanding requirements for channel count and bandwidth," Blankman says. "These standards utilize bit rates of 25 and 28 Gbits/sec. Typically, an oscilloscope with four or five times the fundamental frequency is needed, which corresponds to 50 to 65 GHz. Since InfiniBand and 40/100GBase-R are multilane, acquiring eight, 12, or even more channels at a time is required to fully characterize SI issues." Blankman points to Teledyne LeCroy's LabMaster 10 Zi, with bandwidth out to 65 GHz and a ChannelSync architecture that synchronizes up to 80 channels to operate as a single instrument.

- **Network analyzers.** Network analyzers are important for characterizing crosstalk in multilane systems and revealing the frequency characteristics of the DUT. Anritsu's Goto points out that in order to acquire the best S-parameter data, the vector network analyzer should have broad frequency coverage. He suggests Anritsu's

SIGNAL INTEGRITY AT DESIGNCON

The conference program for DesignCon 2013, which convenes Jan 28–31 at the Santa Clara (CA) Convention Center, is packed with signal-integrity papers and presentations. Here are a few highlights:

- **Tutorial, "Design and Verification for High-Speed I/Os at Multiple to >40 Gbps with Jitter, Signal Integrity, and Power Optimization," http://bit.ly/Xe2PcG;**
- **Panel, "Case of the Closed Eye: A Growing 100G Dilemma," http://bit.ly/12m6F7W;**
- **Session, "High-Throughput, High-Sensitivity Measurement of Power Supply-Induced Bounded, Uncorrelated Jitter in Time, Frequency, and Statistical Domains," http://bit.ly/TPPUwn;**
- **Session, "Understanding Apparent Increasing Random Jitter with Increasing PRBS Test Pattern Lengths," http://bit.ly/TVQyf9.**

VectorStar VNA, which ranges from 70 kHz to 125 GHz.

"While the upper frequency receives most of the attention," he warns, "it is important to remember that accurate measurements to the lowest possible frequency are critical for signal-integrity applications. Often, the accuracy of models can be improved by measuring down to as close to dc as possible, providing the precise data to help create a high-accuracy eye diagram."

Blankman notes that network analyzers with high port counts can be expensive. He says the network analyzers in Teledyne LeCroy's SPARQ series (**Figure 4**) were designed for signal-integrity measurements and offer a lower-cost option to a traditional VNA. (SPARQ stands for "S-parameters quick.")

• **Software.** Given the need for more simulation, vendors are developing software tools to work with their hardware. Loberg notes the availability of serial-data-link analysis (SDLA) on the Tektronix scope (**Figure 5**), which can help engineers simulate equalization in EDA environments such as those from Cadence Design Systems or Mentor Graphics. "That software model can be dropped into an oscilloscope, transferring the model properties into the S-parameters; then we can place the effects of that effort into a filter on the scope," Loberg explains. "The scope can then model the behavior of the equalizer into the signal being measured and see if we can open the eye. This approach allows you to analyze the performance with the effects of equalization baked into the scope."

Teledyne LeCroy also offers oscilloscope-based serial-data-analysis software in its SDAIII-CompleteLinQ product. Blankman notes that it is important to have scope-based software that performs eye, jitter, and vertical noise analysis. He says users also need tool kits that allow fixtures and interconnects to be de-embedded or emulated, and that apply transmitter and receiver equalization. "The analysis tool kit should also provide a wide variety of plots that show the variation and distribution of jitter and noise in frequency and time in order to understand the root causes of noise and jitter," Blankman adds.

• **BERT.** "Receiver testing is becoming mandatory in many standards, and most people don't know where to start," says Howard, who adds that system calibration—critical for ensuring the accuracy of your measurements—may be the hardest part of testing.

Howard reveals that in working with engineers, she has found proper calibration of the stress signal in PCIe 3.0 to be challenging. She points to the Agilent N4903B J-BERT high-performance serial BERT to test Rx compliance. The instrument can characterize a receiver's jitter tolerance and is designed to prove compliance with today's most popular serial-bus standards, including PCIe, SATA/SAS, DisplayPort, and USB.

Goto suggests that when selecting a BERT, engineers should choose one with minimal intrinsic jitter. For example, the Anritsu MP1800A has intrinsic clock jitter of <350 fsec RMS. The BERT should also be able to conduct repeatable and stable jitter-tolerance tests with a variety of generated jitter types, such as sinusoidal, random, and bounded uncorrelated jitter and spread-spectrum clock that can be measured up to 32.1 Gbits/sec.

• **Embedded test.** The days of probing test pads are coming to a close, especially for high-speed buses, because the practice can introduce anomalies into the signal. So where does that leave us? There is a growing interest in embedded test instruments, and the design-for-test movement is allowing nonintrusive embedded instruments to deliver the signal data that the receivers see. "In other words," says Caffee, "soft access is provided to the hard data that signal-integrity engineers need."

Embedded instruments have been used for years for chip-level characterization, verification, and test. But now, embedded instruments are being used to monitor and report data being

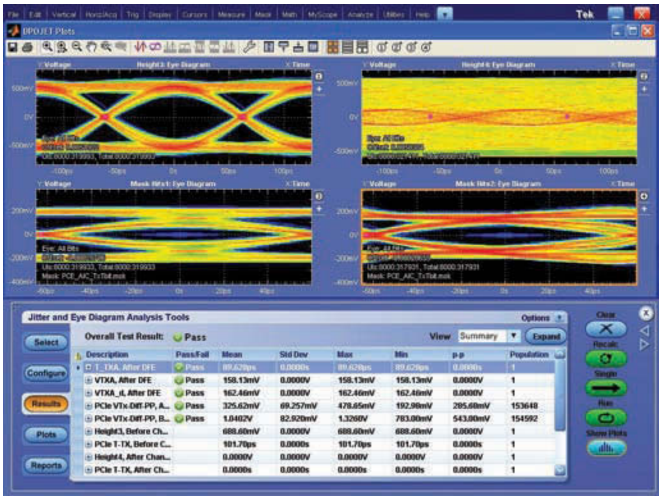

Figure 5 This screen image of serial-data-link analysis shows different eye diagrams before and after inclusion of equalization effects and channel/fixturing effects (courtesy Tektronix).

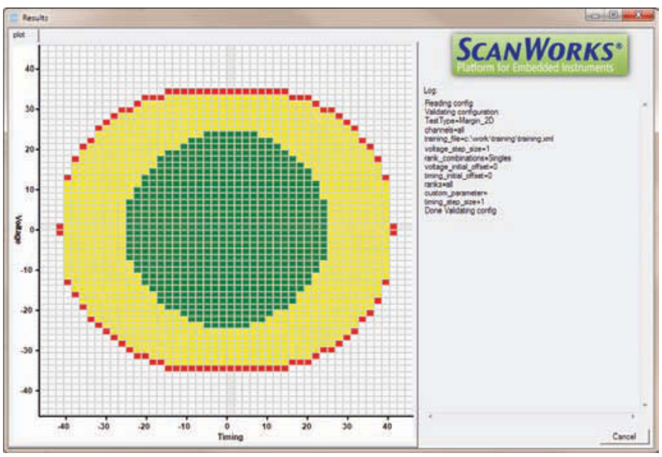

Figure 6 An eye diagram like this one can be generated by a tool set for embedded instrumentation (courtesy Asset InterTech).

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received by the receiver. Caffee notes that the embedded instruments are accessed using standard technologies, such as the IEEE 1149.1 boundary-scan (JTAG) test-access port.

"JTAG provides access to an external software-based platform that can manage the embedded instruments in the system, as well as compile and analyze the test and measurement data they gather," Caffee says (**Figure 6**).

JTAG PROVIDES ACCESS TO AN EXTERNAL SOFTWARE-BASED PLATFORM THAT CAN MANAGE THE SYSTEM'S EMBEDDED INSTRUMENTS.

As system speed and complexity continue to rise, the way forward looks to be a combination of advanced measurement tools and techniques that work with customized simulation models. In the end, though, the path of least resistance for improving signal integrity looks to be an industry standby: good old-fashioned engineering ingenuity. EDN

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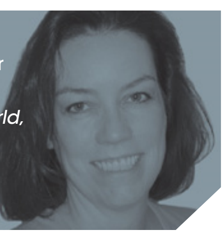


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BY MARK FORTUNATO • MAXIM INTEGRATED

Why your 4.7-μF ceramic cap becomes a 0.33-μF cap

AN INVESTIGATION INTO TEMPERATURE AND VOLTAGE VARIATIONS IN X7R CAPACITORS UNDERSCORES THE IMPORTANCE OF DATA SHEETS.

A few years ago, after more than 25 years of working with ceramic capacitors, I learned something new about them. I was working on an LED-light-bulb driver, and the time constant of an RC circuit in my project simply did not seem to be right.

I immediately assumed that there was an incorrect component value installed on the board, so I measured the two resistors serving as a voltage divider. They were just fine. I desoldered the capacitor from the board and measured that component; the cap, too, was fine. Just to be sure, I measured and installed new resistors and a new capacitor, fired up the circuit, checked that the basic operation was proper, and then went to see whether the component swap had resolved my RC time-constant problem. It had not.

I was testing the circuit in its natural environment: in its housing, which itself was in an enclosure to mimic a "can" for ceiling lighting. The component temperatures in some instances reached well over +100°C. Even in the short time it had taken me to retest the RC behavior, things had gotten quite hot.

My next conclusion, of course, was that the temperature variation of the capacitor was the issue. I was skeptical of that conclusion even as I drew it, however, because I was using X7R capacitors, which to my recollection varied only ±15% up to +125°C. I trusted my memory, but to be sure, I reviewed the data sheet for the capacitor that I was using.

That is when my ceramic-capacitor reeducation began.

BACKGROUNDER

Table 1 shows the letters and numbers used for various ceramic-capacitor types and what each means. The **table** describes Class II and Class III ceramics. Without getting too deep into details, Class I capacitors include the common COG (NPO) type; these are not as volumetrically efficient as the ones listed in the **table**, but they are far more stable over varying environmental conditions, and they do not exhibit piezo effects. The capacitors listed in the **table**, by contrast, can have widely varying characteristics; they will expand and contract with applied voltage, sometimes causing audible (buzzing or ringing) piezo effects.

Of the many capacitor types shown, the most common, in my experience, are X5R, X7R, and Y5V. I never use the Y5Vs, because they exhibit extremely large capacitance variation over the range of environmental conditions.

When capacitor companies develop products, they choose materials with characteristics that will enable the capacitors to operate within the specified variation (third character; **Table 1**) over the specified temperature range (first and second characters). The X7R capacitors that I was using should

TABLE 1 COMMON CERAMIC-CAPACITOR TYPES

First character: low temp		Second character: high temp		Third character: Change over temp (max)	
Char	**Temp** (°C)	**Num**	**Temp** (°C)	**Char**	**Change** (%)
Z	10	2	45	A	±1
Y	30	4	65	B	±1.5
X	55	5	85	C	±2.2
—	—	6	105	D	±3.3
—	—	7	125	E	±4.7
—	—	8	150	F	±7.5
—	—	9	200	P	±10
—	—	—	—	R	±15
—	—	—	—	S	±22
—	—	—	—	T	22, –33
—	—	—	—	U	22, –56
—	—	—	—	V	22, –82

not have varied more than ±15% over a temperature range of –55°C to +125°C, so either I had a bad batch of capacitors or something else was happening in my circuit.

NOT ALL X7Rs ARE CREATED EQUAL

Since my RC time-constant problem was far greater than would be explained by the specified temperature variation, I had to dig deeper. Looking at the data for capacitance variation versus applied voltage for my capacitor, I was surprised to see how much the capacitance changed with the conditions I had set. I had chosen a 16V capacitor to operate with a 12V bias. The data sheet indicated that my 4.7-µF capacitor would typically provide 1.5 µF of capacitance under those conditions. Now, *that* explained the problem my RC circuit was having.

The data sheet then showed that if I just increased the size of my capacitor from the 0805 to the 1206 package size, the typical capacitance under the specified conditions would be 3.4 µF. This called for more investigation.

I discovered that Murata Manufacturing Co (www.murata.com) and TDK Corp (www.tdk.com) offer nifty tools on their Web sites that let you plot the variations of capacitors over different environmental conditions. I investigated 4.7-µF capacitors of various sizes and voltage ratings. **Figure 1** graphs the data that I extracted from the Murata tool for several different 4.7-µF ceramic capacitors. I looked at both X5R and X7R types, in package sizes from 0603 to 1812 and with voltage ratings from 6.3 to 25V dc. Note, first, that as the package size increases, the capacitance variation with applied dc voltage decreases—and does so substantially.

A second interesting point is that, for a given package size and ceramic type, the capacitor voltage rating seems often to have no effect. I would have expected that using a 25V-rated capacitor at 12V would result in less variation than using a 16V-rated capacitor under the same bias. Looking at the traces for X5Rs in the 1206 package, it's clear that the 6.3V-rated part does indeed perform better than its siblings with higher voltage ratings.

If we were to examine a broader range of capacitors, we would find this behavior to be common. The sample set of capacitors that I considered in my investigation did not exhibit the behavior to the same extent as the general population of ceramic capacitors would.

TABLE 2 CAPACITANCE OF X7R CAPS WITH A 12V BIAS

Size	C (µF)	% of Nominal
0805	1.53	32.6
1206	3.43	73
1210	4.16	88.5
1812	4.18	88.9
Nominal	4.7	100

A third observation is that, for the same package, X7Rs have better temperature sensitivity than do X5Rs. I do not know whether this holds true universally, but it did seem so in my investigation.

Using the data from this graph, **Table 2** shows how much the X7R capacitances decreased with a 12V bias. Note that there is a steady improvement with progressively larger capacitor sizes until the 1210 size; going beyond that size yields no real improvement.

CHOOSING THE RIGHT CAPACITOR

In my case, I had chosen the smallest available package for a 4.7-µF X7R because size was a concern for my project. In my ignorance, I had assumed that any X7R was as effective as any other X7R; clearly, this is not the case. To get the proper performance for my application, I had to use a larger package.

I really did not want to go to a 1210 package. Fortunately, I had the freedom to increase the values of the resistors involved by about 5× and thereby decrease the capacitance to 1 µF.

Figure 2 graphs the voltage behavior of several 16V, 1-µF X7R caps versus that of 16V, 4.7-µF X7Rs. The 0603 1-µF capacitor behaves about the same as the 0805 4.7-µF device. Both the 0805 and 1206 1-µF capacitors perform slightly better than the 1210 4.7-µF size. Thus, by using the 0805 1-µF device, I was able to keep the capacitor size unchanged while getting a capacitor that only dropped to about 85% of nominal, rather than 30%, under bias.

But I was still confused. I had been under the impression that all X7R caps *should* have similar voltage coefficients because the dielectric used was the same, namely X7R. So I

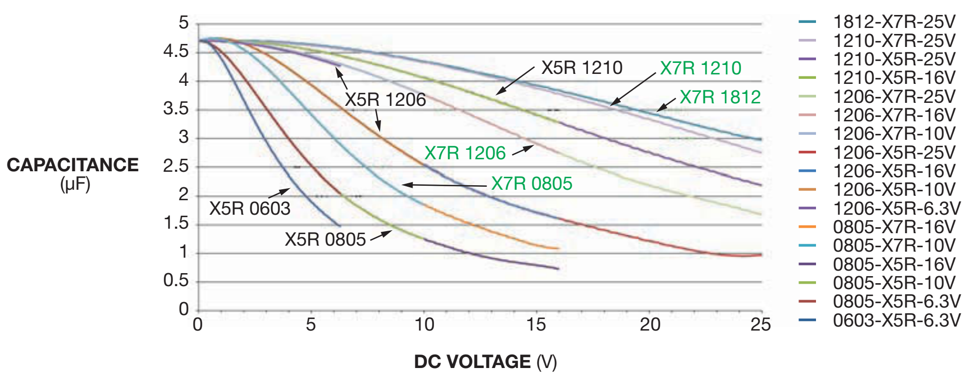

Figure 1 As this graphic representation of temperature variation versus dc voltage for select 4.7-µF capacitors shows, as the package size increases, the capacitance variation with applied voltage substantially decreases.

contacted a colleague and expert on ceramic capacitors, TDK field applications engineer Chris Burkett, who explained that there are many materials that qualify as "X7R." In fact, any material that allows a device to meet or exceed the X7R temperature characteristics, ±15% over −55°C to +125°C, can be called X7R. Burkett also explained that there are no voltage-coefficient specifications for X7R or any other ceramic-capacitor type.

This is a critical point, so I will repeat it. A vendor can call a capacitor X7R (or X5R, or any other type) as long as the cap meets the temperature-coefficient specs, regardless of how bad the voltage coefficient is. This fact reinforces the old maxim (pun intended) that any experienced applications engineer knows: Read the data sheet!

As capacitor vendors have turned out progressively smaller components, they have had to compromise on the materials used. To get the needed volumetric efficiencies in the smaller sizes, they have had to accept worse voltage coefficients. Of course, the more reputable manufacturers do their best to minimize the adverse effects of this trade-off.

Consequently, when using ceramic capacitors in small packages—indeed, when using any component—it is extremely important to read the data sheet. Regrettably, often the commonly available data sheets are abbreviated and will provide little of the information you'll need to make an informed decision, so you may have to press the manufacturer for more details.

What about those Y5Vs that I summarily rejected? For kicks, let's examine a common Y5V capacitor. I chose a 4.7-μF, 0603-packaged capacitor rated at 6.3V—I won't mention the vendor, because its Y5V cap is no worse than any other vendor's Y5V cap—and looked at the specs at 5V and +85°C. At 5V, the typical capacitance is 92.9% below nominal, or 0.33 μF.

That's right. Biasing this 6.3V-rated capacitor with 5V will result in a capacitance that is 14 times smaller than nominal.

At +85°C with 0V bias, the capacitance decreases by 68.14%, from 4.7 to 1.5 μF. Now, you might expect this to reduce the capacitance under 5V bias from 0.33 to 0.11 μF. Fortunately, however, those two effects do not combine in this way. In this particular case, the change in capacitance with 5V bias is worse at room temperature than at +85°C.

To be clear, with this part under 0V bias, the capacitance drops from 4.7 μF at room temperature to 1.5 μF at +85°C, whereas under 5V bias the capacitance increases with temperature, from 0.33 μF at room temperature to 0.39 μF at +85°C. This result should convince you that you really need to check component specifications carefully.

GETTING DOWN TO SPECIFICS

As a result of this lesson, I no longer just specify an X7R or X5R capacitor to colleagues or customers. Instead, I specify specific parts from specific vendors whose data I

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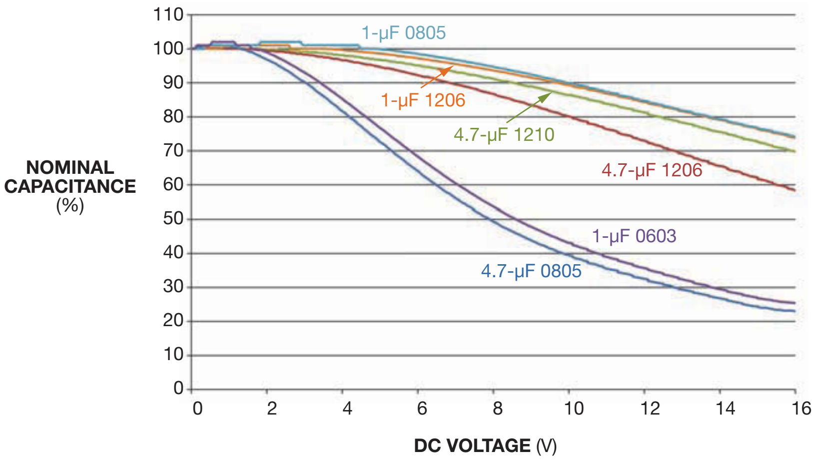

Figure 2 This graph, which plots the voltage performance of 1-µF and 4.7-µF capacitors, shows similar performance for the 1-µF 0603 and the 4.7-µF 0805.

have checked. I also warn customers to check data when considering alternative vendors in production to ensure that they do not run into the problems I encountered.

The larger lesson here, as you may have surmised, is to read the data sheet, every time, without exception. Ask for detailed data when the data sheet does not contain sufficient information. Remember, too, that the ceramic-capacitor designations X7R, Y5V, and so on imply nothing about voltage coefficients. Engineers must check the data to know, really know, how a specific capacitor will perform under voltage.

Finally, keep in mind that, as we continue to drive madly to smaller and smaller sizes, this is becoming more of an issue every day. **EDN**

ACKNOWLEDGMENT

The author thanks Chris Burkett, field applications engineer at TDK, for his explanation of why ceramic capacitors of the same nominal type can have widely divergent voltage coefficients.

AUTHOR'S BIOGRAPHY

Mark Fortunato is senior principal member of the technical staff in the Communications and Automotive Solutions Group at Maxim Integrated (San Jose, CA). He has spent much of the past 16 years helping customers tame analog circuitry. Before that, Fortunato worked on products ranging from speech-recognition systems to consumer electronics, millimeter-wave instrumentation, and automated teller machines. He regrets that he never got to meet Jim Williams or Bob Pease.

DESIGN NOTES

System Monitor with Instrumentation-Grade Accuracy Used to Measure Relative Humidity

Design Note 510

Leo Chen

Because much can be deduced about a physical system by measuring temperature, it is by far the most electronically measured physical parameter. Selecting a temperature sensor involves balancing accuracy requirements, durability, cost and compatibility with the measured medium. For instance, because of its low cost, a small-signal transistor such as the MMBT3904 is an attractive choice for high volume or disposable sensing applications. Although such sensors are relatively simple, accurate temperature measurement requires sophisticated circuitry to cancel such effects as series resistance.

The LTC2991 system monitor has this sophisticated circuitry built in—it can turn a small-signal transistor into an accurate temperature sensor. It not only measures remote diode temperature to ±1°C accuracy, but it also measures its own supply voltage, single-ended voltages (0 to V_{CC}) and differential voltages (±325mV).

While ostensibly designed for system monitor applications, the top shelf performance of the LTC2991 makes it suitable for instrumentation applications as well, such as the accurate psychrometer described here.

A Psychrometer: Not Nearly as Ominous as It Sounds

A psychrometer is a type of hygrometer, a device that measures relative humidity. A hygrometer uses two thermometers, one dry (dry bulb) and one covered in a fabric saturated with distilled water (wet bulb). Air is passed over both thermometers, either by a fan or by swinging the instrument, as in a sling psychrometer. A psychrometric chart can then be used to calculate humidity by using the dry and wet bulb temperatures. Alternatively, a number of equations exist for this purpose. The following equations are used in testing this circuit.

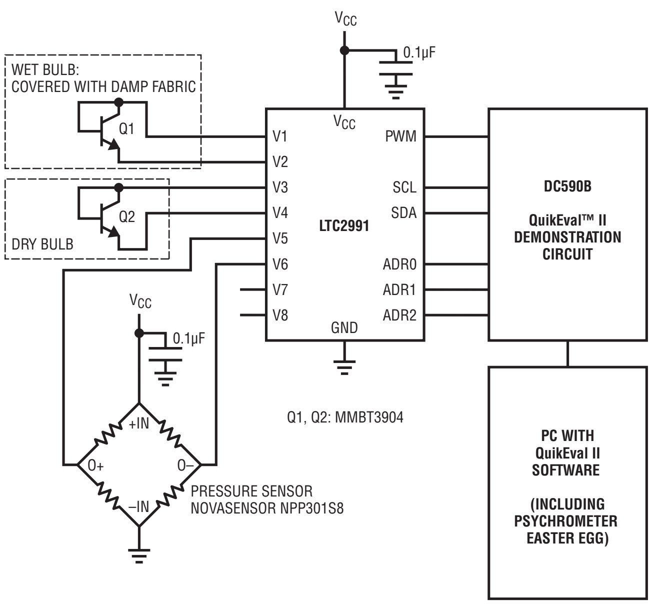

Figure 1. Simple Psychrometer Using the LTC2991

$$A = 6.6 \bullet 10^{-4} \bullet (1 + 1.115 \bullet 10^{-3} \bullet WET)$$

$$ESWB = e^{\left(\frac{16.78 \bullet DRY - 116.9}{WET + 273.3}\right)}$$

Where:

$$ED = ESWB - A \bullet P \bullet (DRY - WET)$$

$$HUMIDITY = \frac{ED}{EDSB}$$

WET = wet bulb temperature in Celsius

DRY = dry bulb temperature in Celsius

P = pressure in kPa

Figure 1 shows a LTC2991-based psychrometer. The two transistors provide the wet bulb and dry bulb temperature readings when connected to the appropriate inputs of the LTC2991.

The equations include atmospheric pressure as a variable, which is determined here via a Novasensor NPP301-100 barometric pressure sensor measured by channels 5 to 6 configured for differential inputs. Full-scale output is 20mV per volt of excitation voltage, at 100kPa barometric pressure (pressure at sea level is approximately 101.325kPa).

The LTC2991 can also measure its own supply voltage, which in our circuit is the same supply rail used to excite the pressure sensor. Thus, it is easy to calculate a ratiometric result from the pressure sensor, removing the error contribution of the excitation voltage.

Error Budget

The LTC2991 remote temperature measurements are guaranteed to be accurate to ±1°C. Figure 2 shows the error in indicated humidity that results from a 0.7°C error in the worst-case direction, and the error in indicated humidity resulting from a 0.7°C error in the worst-case direction combined with worst-case error from the pressure sensor.

Try It Out!

A psychrometer readout is implemented as an Easter egg in the LTC2991 (DC1785A) demonstration software, available as part of the Linear Technology QuikEval software suite.

The demo board should be set up as shown in Figure 1. To access the readout, simply add a file named tester.txt in the install directory of your DC1785A software. The contents of this file do not matter. On software start-up, the message "Test mode enabled" should be shown in the status bar, and a Humidity option will appear in the Tools menu. Relative humidity readings can then be compared to sensors of similar accuracy grade, such as resistive and capacitive film.

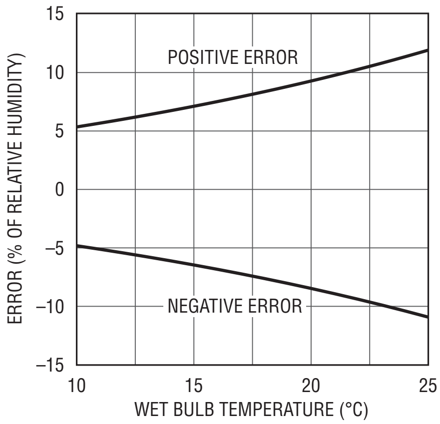

Figure 2. Worst-Case Error

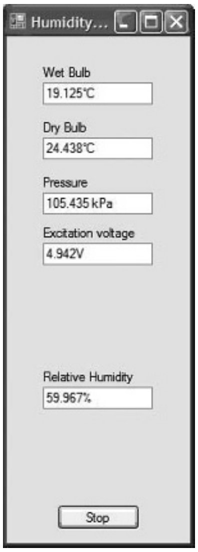

Figure 3. A Psychrometer Readout Is Implemented as an Easter Egg in the LTC2991 (DC1785A) Demonstration Software, Available as Part of Linear's QuikEval Software Suite

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DESIGN NOTES

Complete Battery Charger Solution for High Current Portable Electronics

3.5A Charger for Li-Ion/$LiFePO_4$ Batteries Multiplexes USB and Wall Inputs

Design Note 496

George H. Barbehenn

Introduction

The LTC®4155 and LTC4156 are dual multiplexed-input battery chargers with PowerPath™ control, featuring I^2C programmability and USB On-The-Go for systems such as tablet PCs and other high power density applications. The LTC4155's float voltage (V_{FLOAT}) range is optimized for Li-Ion batteries, while the LTC4156 is optimized for lithium iron phosphate ($LiFePO_4$) batteries, supporting system loads to 4A with up to 3.5A of battery charge current. I^2C controls a broad range of functions and USB On-The-Go functionality is controlled directly from the USB connector ID pin.

Input Multiplexer

A distinctive feature of the LTC4155/LTC4156 PowerPath implementation is a dual-input multiplexer using only N-channel MOSFETs controlled by an internal charge pump. The input multiplexer has input priority selection and independent input current limits for each channel.

Applications include any device with a high capacity Li-Ion or $LiFePO_4$ battery that can be charged from a high current wall adapter input or from the USB input—such as a tablet PC. Figure 1 shows a typical application and Figure 2 shows its efficiency.

This dual input multiplexer implementation allows the use of inexpensive, low $R_{DS(ON)}$ N-channel MOSFETs. The MOSFETs also provide overvoltage protection (OVP) and if desired, backdrive blocking and reverse-voltage

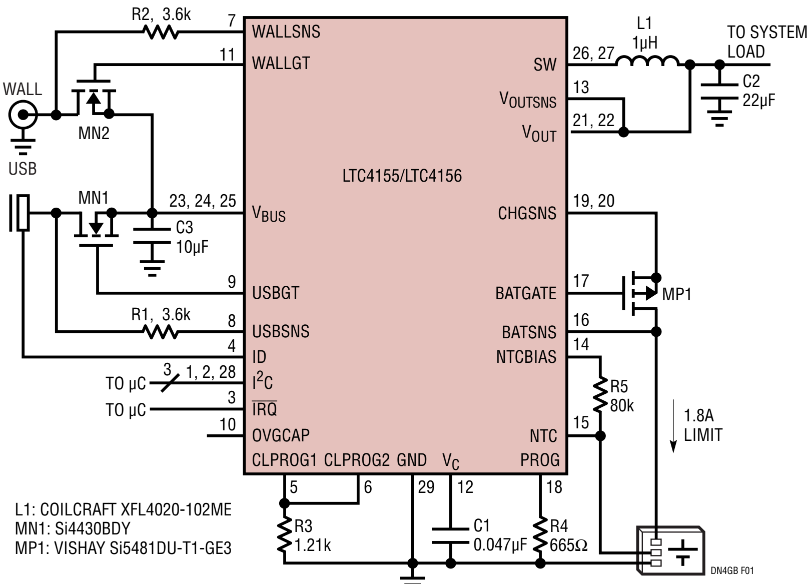
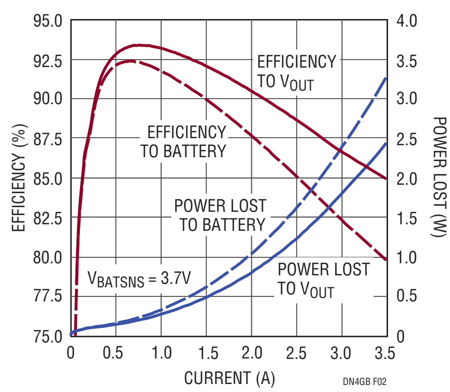


Figure 1. Typical Application Using a Simple Input Multiplexer with No Backdrive Protection



INCLUDES LOSSES FROM 2× Si7938DP OVP FETS XFL4020-102ME INDUCTOR AND Si5481DU CHARGER FET

Figure 2. Switching Regulator Efficiency

protection (RVP). Backdrive blocking prevents voltage on the wall input from backdriving the USB, or vice-versa. Backdrive blocking can be implemented on one or both inputs. Reverse-voltage protection prevents a negative voltage applied to the protected input from reaching downstream circuits.

Dual High Current Input Application

Figure 3 shows a dual 3.5A input application, featuring OVP, RVP and backdrive protection. The FDMC8030 MOSFETs provide ±40V of OVP and RVP protection.

0V~6V Input on Either WALL or USB

In the circuit of Figure 3, when a 0V~6V input is present on either input, the corresponding gate signal rises to approximately twice V_{IN}, enabling the two series N-channel MOSFETS and connecting the input to V_{BUS}. The undervoltage lockout (UVLO) is approximately 4.35V on each channel.

The LTC4155/LTC4156 have an input priority bit, which defaults to WALL. If a valid voltage is present on both inputs, only WALLGT is activated. The input priority bit can be changed via I^2C to make the USB channel preferred when both inputs are present.

>6V Input on Either WALL or USB

When either input goes above 6V, the corresponding WALLGT or USBGT pin is pulled low, shutting off the corresponding MOSFETs and disconnecting the input. If both inputs have 5V on them, and the input that is enabled by the input priority bit goes above 6V, the LTC4155/LTC4156 automatically and seamlessly switches to the other input—with no disturbance on V_{OUT}.

The diode-connected NPNs (Q3 and Q4) serve to prevent excess V_{GS} on the MOSFET closest to the input of the corresponding channel current from the input flows through the diode, through the B-C junction of the NPN bipolar transistor, and pulls the gate up through the 5M resistor. This prevents the gate from dropping below the source by more than 2V.

A voltage greater than 6V on one input does not prevent the other input from operating normally.

< 0V Input on Either WALL or USB

The USBSNS and WALLSNS pins ignore any negative inputs, but clamp the pins to $–V_F$ (about –0.6V). The negative voltage forward-biases the base-emitter junction of the NPN bipolar transistor, shorting the gate to the input and ensuring that the gate is never more than about 0.5V above the source.

A negative voltage on one input does not prevent the other input from operating normally.

OTG Operation

The LTC4155/LTC4156 drive the USBGT pin high when USB On-The-Go operation is enabled, connecting V_{BUS} to the USB input and enabling up to 500mA to be sourced.

Conclusion

The LTC4155/LTC4156 implement an overvoltage and reverse-voltage protected, prioritized input multiplexer for products that need to support multiple system power or battery charging functionality. Optional backdrive blocking prevents the appearance of voltages at an unconnected input.

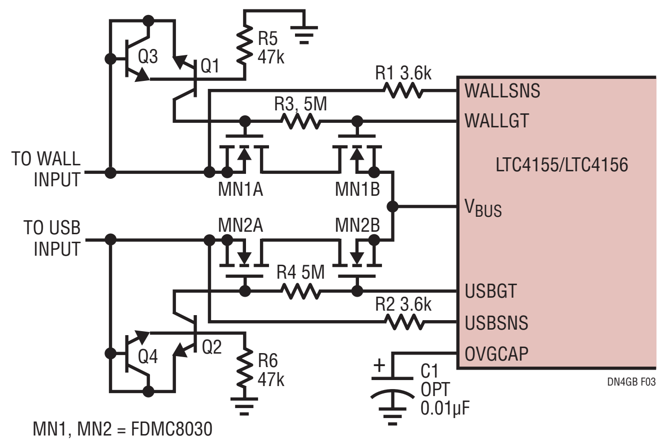


Figure 3. LTC4155/LTC4156 Input Multiplexer with OVP, RVP and Backdrive Blocking

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An improved offline driver lights an LED string

Yan-Niu Ren, Southwest Petroleum University, Chengdu, China

A constant current is better than a constant voltage for driving LEDs. In this proposed circuit, a common constant-voltage regulator is changed into a constant-current source for LEDs. In addition, a startup current limiter is used to suppress large current surges, and a voltage chopper is employed for a wide ac input of 96 to 260 V_{RMS}.

THIS APPROACH MINIMIZES CCR POWER DISSIPATION WHILE KEEPING LED CURRENT CONSTANT.

The concept presented here originates from two Design Ideas published in 2011 (**references 1** and **2**) and was developed to improve power efficiency at a low cost. The circuits shown in **figures 1** and **2** both have the same brilliance of an inductorless chopper and the same controversial issue of power efficiency. To improve the power efficiency, you should observe two principles: The resistors of the chopper should dissipate as little power as possible, and the chopper should switch at the appropriate threshold voltage, V_{TH}. In addition, V_{TH} should be as close as possible to the operating voltage across the LED string. This approach minimizes the power dissipation of the constant-current regulator (CCR) while maintaining a constant LED current.

The circuit shown in **Figure 3** is an example that follows the principles described above, with a power efficiency of about 85%. Voltage regulator IC_1 and R_5 form a 20-mA CCR. The LED string has a sufficient number of LEDs to require 120V at 20 mA. The voltage across R_6 provides a means for indirect measurement of the LED current.

V_{TH} is the diode bridge full-wave rectified output voltage above which, when divided by R_1 to R_3, the 68V bias of D_5 is overcome, turning on Q_1 and turning off Q_2. C_1 charges quickly to V_{TH} while Q_2 is on, then discharges slowly

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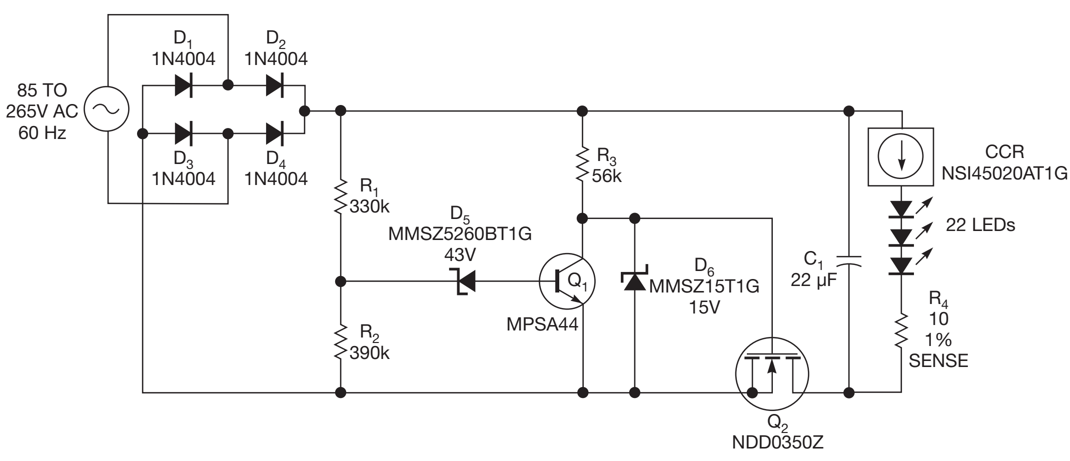


Figure 1 This circuit drives a string of LEDs with a constant current over the entire worldwide range of ac-mains voltages. The resistor in series with the LED string provides a convenient point to measure LED current via its voltage drop.

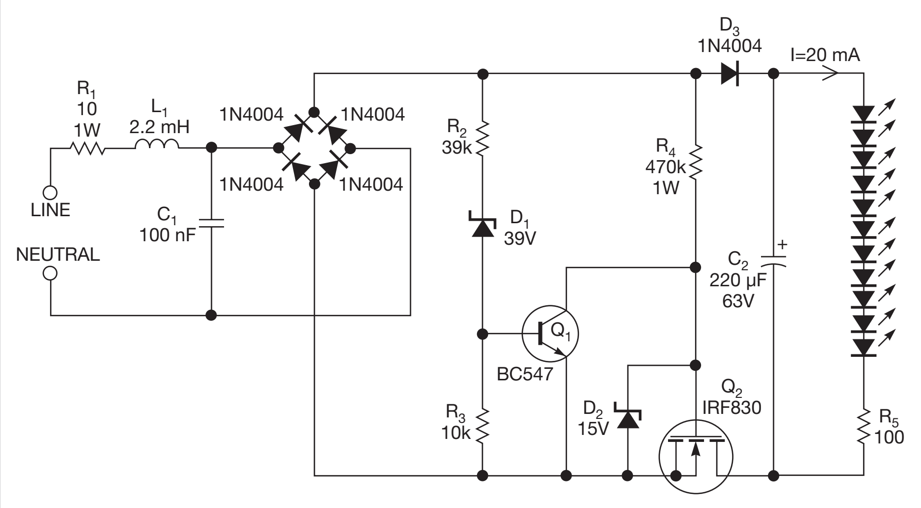


Figure 2 The chopper operation is similar to the circuit of Figure 1; the larger LED series resistor, instead of a constant-current source, provides the current-limit function.

TABLE 1 POWER EFFICIENCY OF IMPROVED CIRCUIT					
V_{RMS} ac at 50 Hz	96	140	180	220	260
Power efficiency (%)	90	87	86	85	82

into the LED string until the next half-cycle of the incoming ac.

V_{TH} must be no less than required to maintain the LED operation voltage of 120V at the end of C_1's discharge and no more than 1.414 times the V_{RMS} of the lowest ac level. With 120V required for the LEDs, plus the 3V input-to-output differential required by IC_1, plus 1.25V developed across R_5, the minimum C_1 voltage will be 124.25V. For simplicity, this figure can be rounded up to 125V.

As shown in **Figure 4**, the C_1 discharge time is much longer than the charge time during a 50-Hz half-cycle of 10 msec. During this period, the peak-to-peak voltage across C_1 is almost 20 mA×10 msec/22 µf=9.09V. Thus, U_{C1_MAX}=125V+9.09V=134.09V. For simplicity, this result can be rounded up to 135V. This is V_{TH}; any voltage above this turns Q_1 on and gets chopped off by Q_2.

When Q_1 switches on, the power consumption of R_4 in **Figure 3** is less than 20 mW at 260V_{RMS} input, and the R_1-R_2-R_3-D_5 divider dissipates less than 100 mW. This result is almost negligible compared with the 2.4W consumed by the LEDs. These resistors are large value so as to consume as little power as possible. R_3 allows fine adjustment of V_{TH} to match the actual drop across the LED string.

A startup current limiter has been included to limit the large inrush current surge through C_1 and Q_2 that would occur if the ac were switched on at a time in its cycle just before V_{TH} was reached. A current-limiting resistor would reduce efficiency on every cycle, but R_9 limits only the surge to 1.35A at power-up until C_2 charges sufficiently to turn on Q_3.

As the ac input increases, the power consumption of the chopper rises a little and power efficiency decreases somewhat, as shown in **Table 1**.

This improved circuit can run at 96V to 260V ac (at 50 Hz). For a larger LED current, increasing the capacity of C_1 and decreasing the resistance of R_5

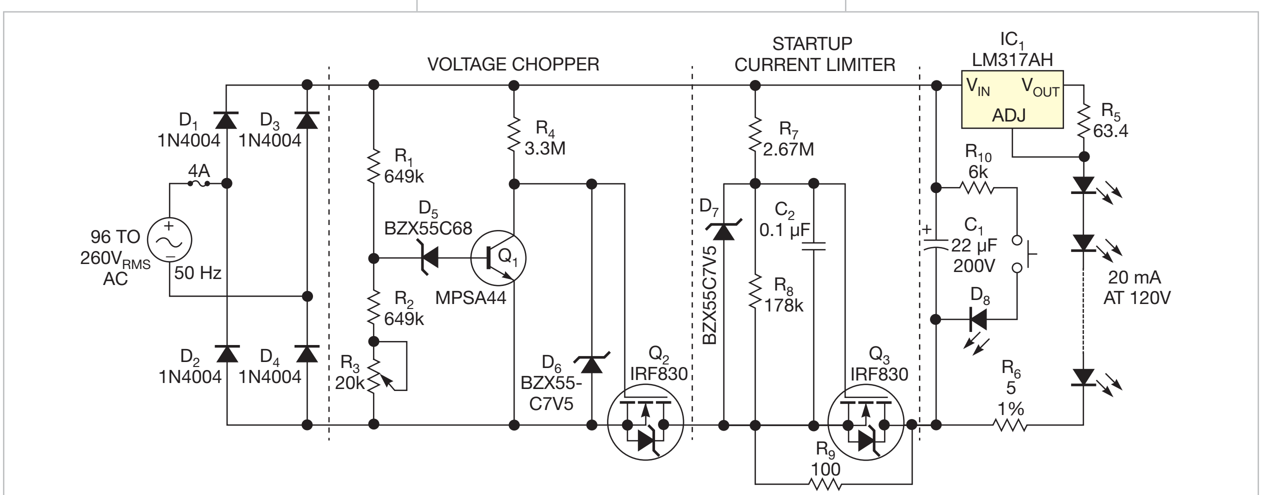
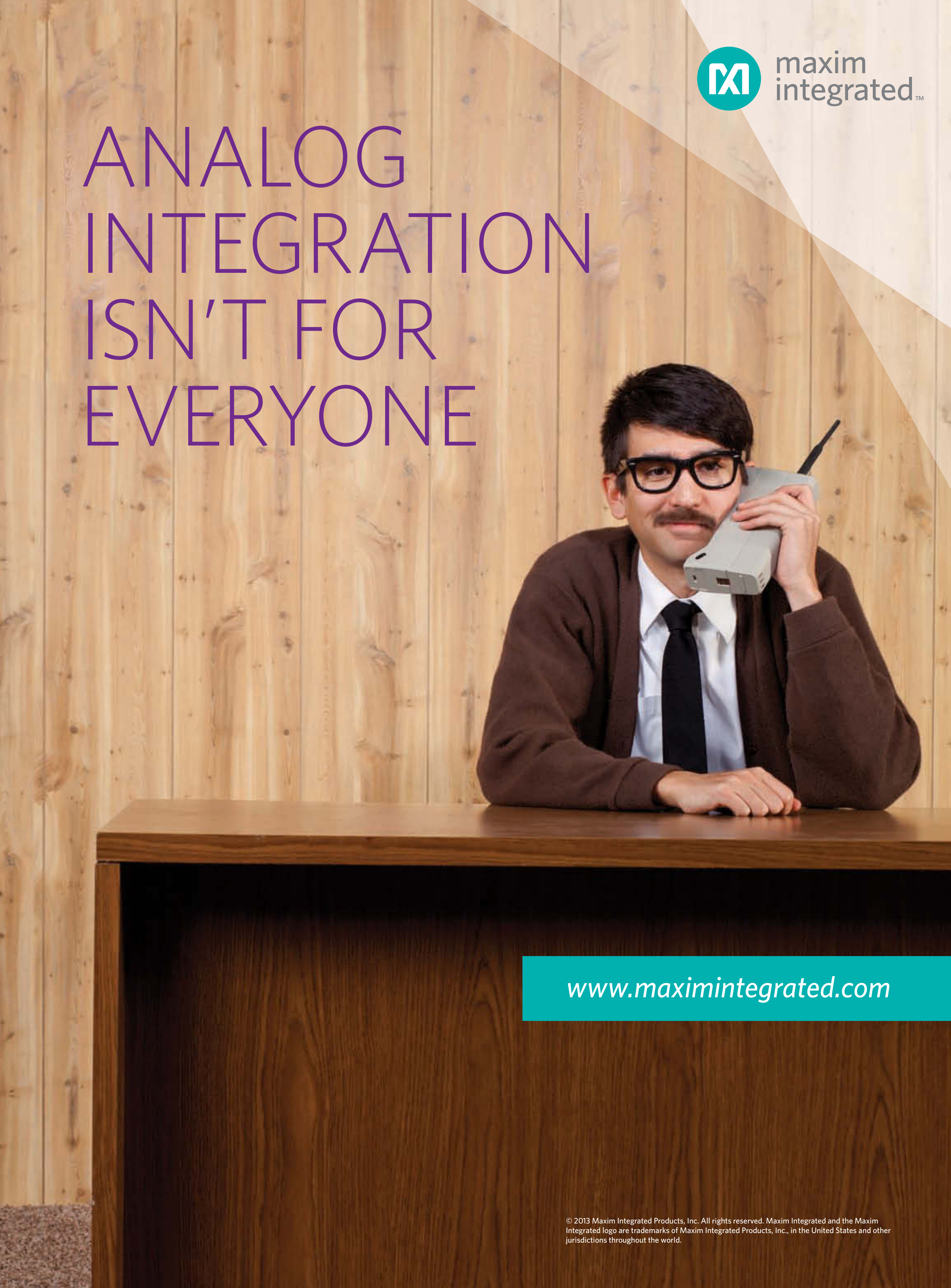


Figure 3 This circuit achieves an efficiency improvement by using tight control of the switching threshold to provide just barely enough LED voltage.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are suggested. For a different LED operation voltage, some parameters should be recomputed in the same way as in the foregoing analysis. The lower the LED operation voltage is, the lower the ac input voltage can be. This Design Idea can also apply to ac at 60 Hz.

Author's notes:

1. Use high-voltage through-hole resistors or series surface-mount resistors to achieve at least 400V withstand. A fuse is suggested for safety against shorts.
2. Safety warning for novice experimenters: Lethal voltages are present in this circuit; use caution when testing and operating it. If scoping, use an isolation transformer to float the circuit's ac input from earth ground; do not float the oscilloscope chassis. The scope ground cannot be connected to the circuit without isolation.
3. Do *not* push the button with ac voltage applied. For safe maintenance, keep pressing the button to discharge C_1 through R_{10} until D_8 goes out. **EDN**

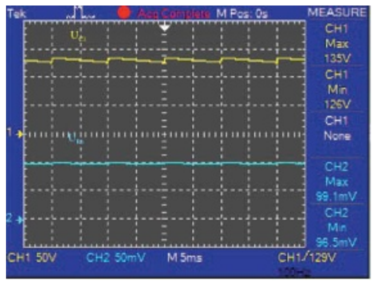


Figure 4 The yellow and blue traces, respectively, present the voltage across C_1 and R_6 in the circuit at $220V_{RMS}$ (at 50 Hz ac). The two traces remain at the same position when the ac input changes from $96V_{RMS}$ to $260V_{RMS}$.

REFERENCES

1 Sheard, Steve, "Driver circuit lights architectural and interior LEDs," *EDN*, Aug 11, 2011, pg 41, www.edn.com/4368306.

2 Babu, TA, "Offline supply drives LEDs," *EDN*, April 21 2011, pg 58, www.edn.com/4369648.

Low-duty-cycle LED flasher keeps power draw at 4 mW

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

Battery-operated equipment often will benefit from a power-on indicator. The indicator, however, can waste significant power. In situations where a low-duty-cycle blinking indicator provides an adequate indication of the power being turned on, the simple circuit described here should prove useful.

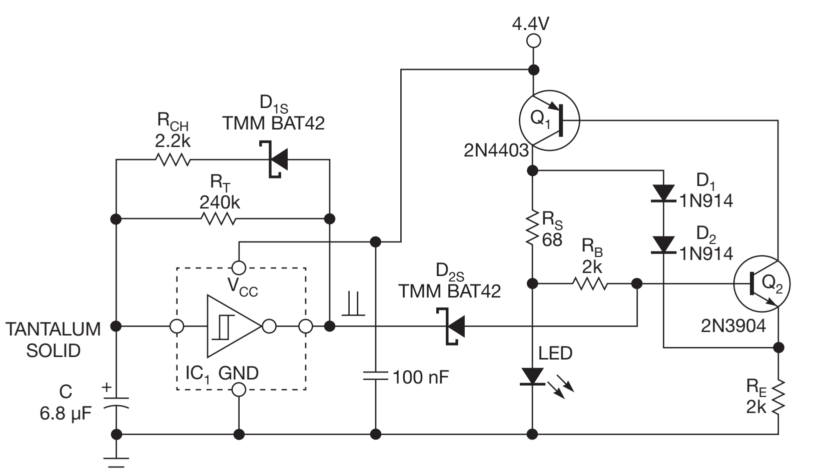
A tiny, single-gate Schmitt-trigger logic inverter, the SN74AHC1G14, together with two resistors, a Schottky diode, and a capacitor form the timing generator of the blinker, shown in **Figure 1**. The output waveform has a period of about 0.5 sec and a very low duty-cycle value, of around 1%. The interval of low-output duration, T_L, of the generator is expressed as

$$T_L = R_T C \times \ln\left(1 + \frac{2}{\frac{V_{CC}}{V_{HYST}} - 1}\right),$$

where V_{HYST} is the hysteresis voltage at the input of IC_1 and V_{CC} is the supply voltage of IC_1.

For V_{CC}=4.5V, the typical value for V_{HYST} is 0.75V. For the required value of T_L=0.5 sec, a value for R_T of 200k was selected. The value of the timing capacitor, C, can be calculated from the **equation**, with a small amount of algebraic rearranging, as 7.45 µF. The nearest standard value is 6.8 µF; a tantalum solid-electrolytic capacitor is used for this value. To achieve the low duty cycle of the generator, the high-output duration, T_H, is shortened by speeding up the time to charge capacitor C. This is done through the additional resistor, R_{CH}, and the series-connected Schottky diode, D_{1S}. The forward voltage drop at D_{1S} is no more than 200 mV and can be neglected. The LED is on for approximately $(1/100)\times T_L \approx 5$ msec.

The LED driver comprises a



NOTE: LED IS A HIGH-RADIANCE TYPE.

Figure 1 Q_1 and Q_2 function as a current source and push a constant current through the LED regardless of its forward voltage drop (within the compliant voltage limitations). The Schmitt inverter forms a classic square-wave generator, modified with R_{CH} and D_{1S} to produce an asymmetrical output.

PNP bipolar transistor, Q_1, and an NPN bipolar transistor, Q_2. Q_1 and Q_2 form a switchable current source. At a high logic level at the cathode of Schottky diode D_{2S}, a constant current flows through the LED with a value of roughly $I_O \approx 0.7V/R_S$, or about 10 mA in this circuit.

Series-connected silicon diodes D_1 and D_2 provide strong nonlinear negative feedback. If for any reason the voltage drop across the sensing resistor, R_S, rises, the D_1-to-D_2 connection will force almost the same increase in voltage at the emitter of Q_2. This increase reduces the collector current of Q_2 and, therefore, the base current of Q_1 and closes the loop; the net result is a reduction of the collector current of Q_1 to maintain a constant value.

Note that when the output of IC_1 goes low, the current through D_{2S} and resistor R_B is negligible. This is due to the fact that, with the output of IC_1 low, the base of Q_2 is held low, turning it and the current source off. With the current source off, the LED is off as well, and only microamps of leakage current flow through D_{2S} and R_B. If you use all surface-mount devices, you can build the circuit on a board no larger than 16×16 mm.

This work was supported by the Slovak Research and Development Agency under contract no. APVV-0062-11. EDN

Rotary encoder with absolute readout offers high resolution and low cost

Michael Korntheuer, Vrije Universiteit Brussel, Brussels, Belgium

Rotary encoders are typically used in positioning systems with servo feedback in which the cost of the encoder usually is of minor importance. Encoders, however, are also used in user interfaces to encode the positions of knobs—the volume knob on an audio system, for example. For those knobs, you have the choice between either a potentiometer boasting low cost, high resolution, and absolute readout but only limited travel—typically less than 340°—or a mechanical-optical rotary encoder, which has endless travel but a higher cost, low resolution, and only relative readout. The Design Idea presented here attempts to combine the advantages of the potentiometer with the endless operation of the mechanical-optical rotary encoder.

The encoder uses standard potentiometer construction techniques and is thus easily produced. It basically is a dual-wiper quadrature endless pot. It consists of a full ring of resistive material, which is powered from opposite sides and on which two electrically independent wipers move. The wipers are mechanically connected to each other at an angle of 90° (**Figure 1**).

An ADC on a microcontroller reads out the two signals; firmware uses both signals to determine in which quadrant the axis is located. Once the quadrant is known, the signal of both wipers can be used to calculate the position of the axis. When a wiper reaches the top or bottom power connections, its signal should be ignored because of nonlinear response (**Figure 2**). Both wipers cannot be in this nonlinear position at the same time because of the 90° angle between the wipers. Today, even the most basic microcontrollers offer a 10-bit ADC, so the combined signals give an 11-bit resolution, or better than 0.2°. The microcontroller can ignore the absolute readout if the application does not require it or when a software reset is useful.

This quadrature endless pot provides a user experience similar to the old tuning knob of a classical analog radio. It offers new possibilities in human-interface design and can give a quality feel in consumer products at low cost. EDN

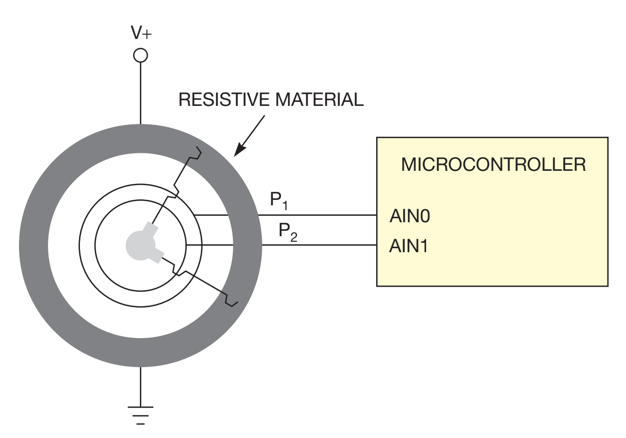


Figure 1 The encoder is a dual-wiper quadrature endless potentiometer that consists of a full ring of resistive material, which is powered from opposite sides and on which two electrically independent wipers move.

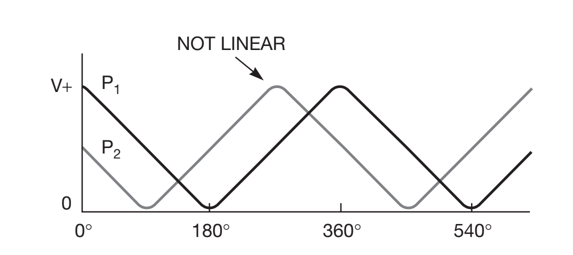


Figure 2 When a wiper reaches the top or bottom power connections, its signal should be ignored because of nonlinear response.

Two-IC circuit combines digital and analog signals to make multiplier circuit

Rick Mally, Independent Designs LLC, Denver

The circuits presented here use an analog switch—such as a DG419 or one-third of a CD4053—to combine an analog signal with a standard PWM signal. Most microcontrollers can easily generate the PWM signal. Combining the PWM signal with the analog signal and lowpassing the result effectively multiplies the analog signal by a digital value. Such a circuit can be useful in signal processing, power factor correction, automatic gain control, and sensor interfacing. All four circuit variants rely on the same principle: using the analog switch to adjust the duty-cycle ratio between two analog input levels, and a lowpass filter (LPF) to eliminate the PWM chopping frequency.

Figure 1a depicts a multiplier incorporating a second-order Sallen-Key LPF. The active filter provides the best ac performance, effectively eliminating the chop frequency and passing slower ac signals through with minimal attenuation. Since the analog switch is selecting either the analog input signal or ground, the output voltage is equal to V_{IN}×D, where D is the duty cycle of the PWM signal; its value ranges from 0 to 1.

Figure 1b shows a variation of this circuit. Using the switch node formerly grounded as an additional analog input produces a circuit that gives an output equal to (A×D)+(B×(1–D)). The PWM duty cycle selects the ratio between the two input signals and presents the result at V_{OUT}.

The filter cutoff frequency should be optimized for the PWM frequency used. The values depicted provide a ~10-kHz cutoff frequency. This should be satisfactory in most applications for an 8-bit PWM clocked at 16 MHz (a PWM frequency of 62.5 kHz). Response time will be less than 200 μsec; noise will be less than 1 LSB. The cutoff frequency can be easily changed by adjusting R_1 and R_2, or C_1 and C_2. It is important that R_1=R_2 and C_2≈0.5×C_1. Doubling the resistor or capacitor values will halve the cutoff frequency; halving them will double the frequency.

LOWPASSING EFFECTIVELY MULTIPLIES THE ANALOG SIGNAL BY A DIGITAL VALUE.

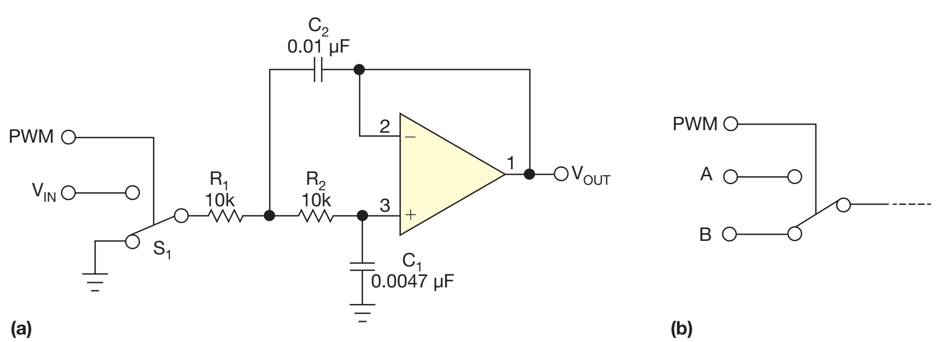


Figure 1 The use of an analog (CMOS) SPDT switch and an op amp configured as an LPF forms a simple multiplier circuit that can be used as either a digitally controlled gain block (a) or a cross-fader (b).

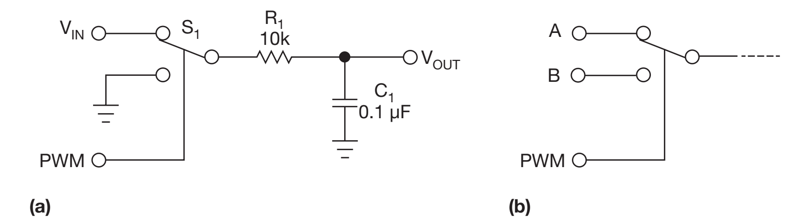


Figure 2 The active two-pole LPF can be replaced with a simpler single-pole passive circuit when slower response times are acceptable. Again, depicted are a gain block (a) and a cross-fader (b).

Figures 2a and **2b** show a simpler version of the previous circuits; they have a much slower response, however, and hence are useful only for generating a dc voltage or a low-frequency ac signal. Again, the roll-off of the LPF should be optimized to block the PWM frequency. For the 8-bit PWM frequency described earlier, the depicted 10k and 0.1 μF provide a response time of 5-msec and less than 1 LSB of noise.

Since all of the circuit variations have a dc gain of 1, the discrete component values affect ac performance only. These circuits are capable of high dc precision without the use of expensive precision components. EDN

Originally published in the Aug 6, 1992, issue of *EDN*

Current loop transmits ac measurement

Mark Fazio, David Scott, and Bob Clarke, Analog Devices, Wilmington, MA

Process-control applications use current loops to send information as an analog signal over long distances with high noise immunity. Using the three-chip circuit in **Figure 1**, you can measure alternating current or voltage and transmit the results on a 4- to 20-mA current loop. The circuit accepts a 0- to 10-mV ac RMS input and provides a 4- to 20-mA output.

The input signal creates a floating voltage across sensing resistor R_{SENSE}, whose size produces 0 to 10 mV RMS from the expected sensed current. This floating voltage is the input to a differential-input, single-ended AD22050 sensor interface, IC_1.

IC_1 operates at a gain of approximately 20 and drives the low-impedance (8-kΩ) input (pin 1) of the AD736 RMS-to-dc converter (IC_2). This converter's full-scale range is 200 mV RMS. IC_2's output drives IC_3, an AD694 voltage to 4- to 20-mA current-loop interface.

Because of their low power consumption, both IC_1 and IC_2 can operate from the 10V supplied by IC_3's reference output at pin 7. IC_3, and hence the entire circuit, operates from the standard 24V loop supply. Because this circuit operates from a single supply, you must bias IC_2's common input at one-half of IC_3's 10V output, or 5V. The voltage divider comprising R_1 and R_2 divides the 10V to 5V. R_2 is in parallel with a 10-kΩ resistor inside IC_3.

IC_3's internal buffer amplifies the difference between IC_2's output at pin 6 and the 5V rail. This difference ranges from 0 to 200 mV dc for a 0- to 10-mV RMS input and produces a 4- to 20-mA current output from IC_3. R_3 allows you to adjust the circuit's gain. R_4 and R_5 set the gain of IC_3's internal amplifier to 10. R_5 matches R_4 to prevent offsets due to the internal amplifier's input-bias current. This circuit's accuracy is 1.2% of readings from 20 Hz to 40 Hz and 1% of readings from 40 Hz to 1 kHz. The −3-dB bandwidth is 33 kHz. EDN

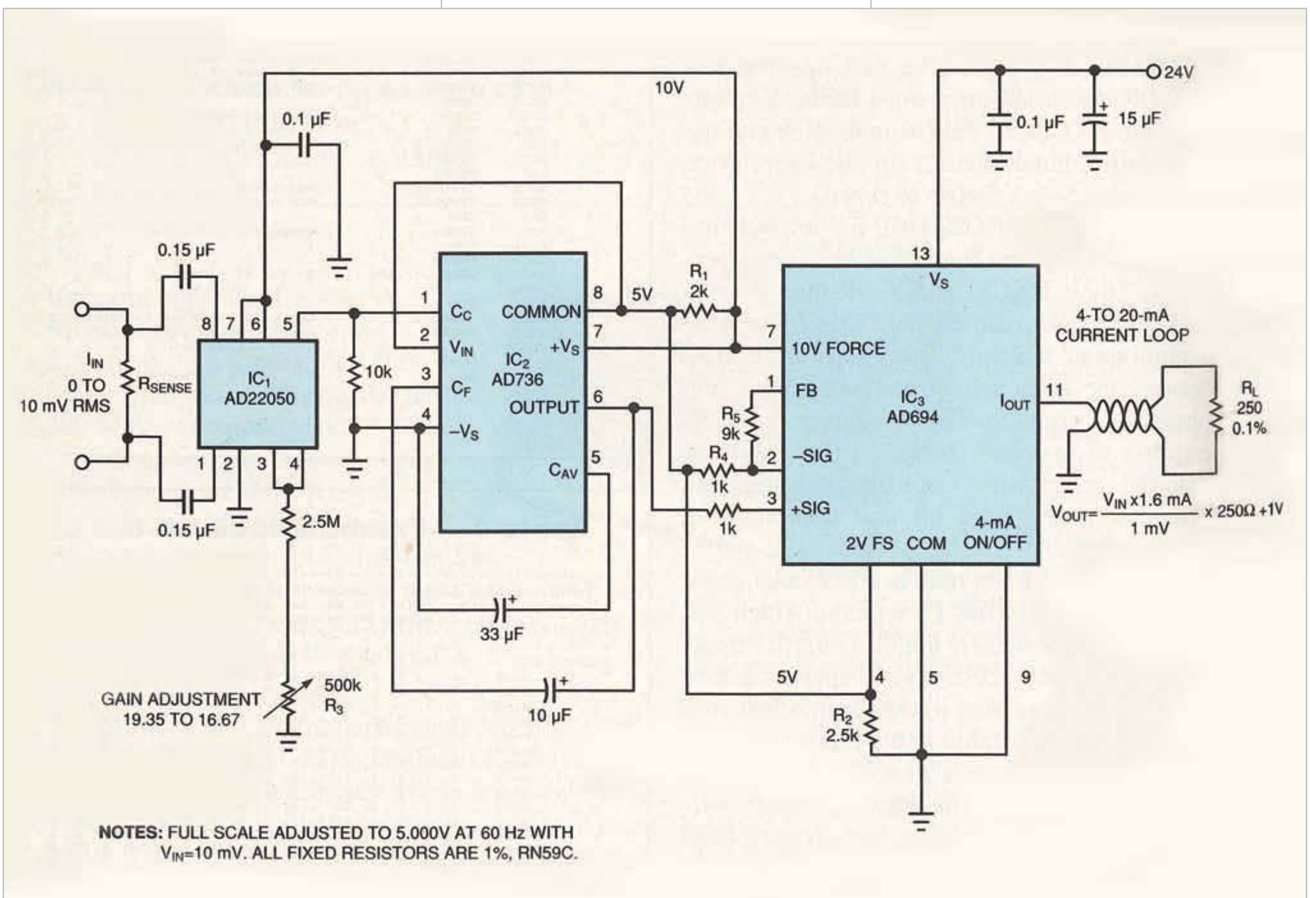


Figure 1 This circuit measures alternating current or voltage and transmits the results on a 4- to 20-mA current loop.

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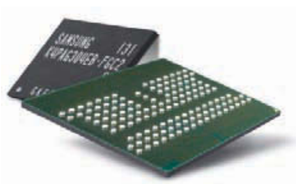
Stability at last for the DRAM market?

A tectonic shift from PCs to mobile devices is remaking the DRAM market, moving a historically volatile business onto firmer, safer ground.

Since the 1980s, DRAM has been a high-volume, commodity business, with the lion's share of production going to PCs. Supply and demand have often been wildly out of balance. A PC market boom would cause DRAM shortages, forcing memory makers to increase production and jacking up DRAM prices. Then the business would crash as supply caught up with—and overshot—demand.



> Mobile DRAM is built to order; production meets demand and generates higher margins.

The rise of mobile devices, however, is changing that cycle. Today's DRAMs fall into one of three major categories: traditional DRAM for PCs (DDR3), DRAM for mobile (low-power DDR2), and specialty DRAM, manufactured for higher performance in particular niches, notes Michael Howard, senior principal analyst for DRAM and compute platforms at IHS Corp. The categories are generally not interchangeable; you can't use PC DRAMs in smartphones and tablets.

And mobile-DRAM demand is rising rapidly. Smartphone sales surpassed PC demand in the fourth quarter of 2011, according to market-research firm Canalys. IDC predicted that mobile devices as a whole would outsell PCs by more than two to one in 2012. According to IHS, PCs accounted for less than half of the DRAM market in the second quarter of 2012—the first time their share had ever fallen below 50%.

The shift has already made a difference in who has survived the brutal DRAM market of the last few years. Mobile DRAM and specialty DRAM are not commodity products, so companies that make those memories in addition to traditional DRAM have seen more stable pricing.

"Mobile DRAM is built to order," says IHS's Howard. "Prices are negotiated quarterly." That means production is more likely to meet demand—and to generate higher margins.

By the end of 2013, the DRAM industry will have shrunk to only three major players, says Howard: Samsung, SK Hynix, and Micron Technology. Other DRAM makers exist, he adds, but they don't own the technology and must license it from those three.

The DRAM vendor in the best position is Samsung, which holds about 40% of the overall DRAM market and 60% of the mobile-DRAM market, according to Howard. It also has a stable customer: itself, in Samsung Mobile. Hynix SK holds 22% to 24% of the overall DRAM market and the same share of the mobile-DRAM market. Micron historically has accounted for about 13% of the overall DRAM market and only 4% of mobile DRAM. It is addressing that situation by acquiring Elpida, which holds about a 20% market share in mobile DRAM.

With the right balance of PC, mobile, and specialty DRAM, these companies should find themselves in a more stable market. All three make NAND flash as well as DRAM. NAND is made in different fabs, says Howard, but if the vendors see too much capacity in DRAMs, they can shift their DRAM fabs to NAND production.

The NAND market has some of the elasticity of the old DRAM market, in that OEMs can always stuff more memory into their products. But while that's true for the solid-state-drive market, says Howard, the mobile-device market lacks similar flexibility; once a smartphone or tablet is designed, it's not a simple task to add more NAND.

Taken together, these factors should help the remaining memory companies build a better business future.

—by Tam Harbert

This story was originally posted by EBN: http://bit.ly/TOO1B3.

OUTLOOK

OEMs TO REDUCE NUMBER OF CONTRACT MANUFACTURERS

Citing increased pressure to maintain profitability and streamline operations, more than half of all electronics OEMs worldwide plan to reduce the number of contract manufacturers they work with during the next year, according to the results of a late-summer 2012 survey conducted by market-intelligence firm IHS iSuppli.

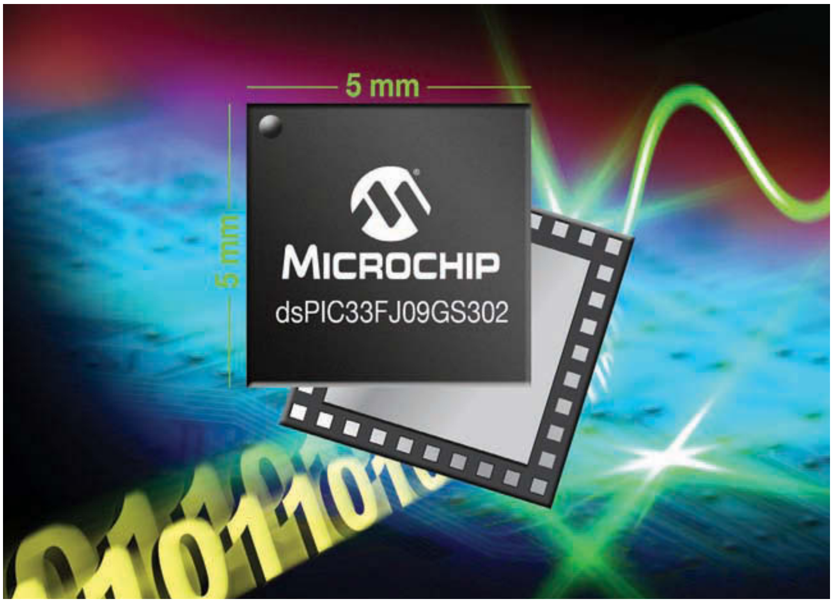
"While the impact of this trend is still to be determined," says Thomas J Dinges, CFA, senior principal analyst for EMS and ODM research at IHS, "such a move by OEMs potentially could result in a reduction in the number of electronics manufacturing services, original design manufacturers, and joint design manufacturers competing in the outsourced-manufacturing business."

On average, each OEM now works with eight outsourced manufacturing partners spanning electronics-manufacturing-service-, original-design-manufacturing, or joint-design-manufacturing-type engagements, or all three, according to the survey. Changes that OEMs say they want to make with their current providers during the next six months are lead-time reduction and price negotiation.

—by Amy Norcross

productroundup

MICROCONTROLLERS



Microchip expands digital-signal-controller lineup with lower-cost options

Microchip Technology Inc's dsPIC33FJ09GS302 family of dsPIC33 GS series digital signal controllers extends its dsPIC DSC portfolio, adding lower-cost options for digital-power conversion. The family enables higher efficiency in ac/dc and dc/dc power supplies, high-intensity-discharge and LED lighting, solar inverters, and other power-conversion applications. The five-member family is optimized for digital-power applications via integrated high-speed ADCs; a zero-wait-state signal-processing core; and flexible, high-resolution PWMs. The new DSCs offer the lowest power dissipation of any of the GS family members and are the first available in a 20-pin SSOP and the smaller 36-pin VTLA package, which has a 5×5-mm footprint. Volume prices (5000) range from \$2.17 to \$2.56. The MPLAB Starter Kit for Digital Power, Part No. DM330017, sells for \$129.

Microchip Technology, www.microchip.com

NXP ultralow-power wireless family targets the Internet of Things

NXP Semiconductors has announced the JN516x family of ultralow-power wireless microcontrollers for JenNet-IP, ZigBee, and other IEEE 802.15.4 applications using NXP 802.15.4-based software stacks. Designed for use within the Internet of Things, the MCUs are intended for applications ranging from smart lighting and home automation to wireless sensor networks. The new devices integrate an MCU; a 2.45-GHz radio; analog peripherals; and up to 256 kbytes of flash, 4 kbytes of E^2PROM, and 32 kbytes of RAM. The MCUs support in-packet antenna diversity, which lets systems choose the best antenna on every packet received. Currently sampling with lead customers, JN516x evaluation kits and chips are scheduled to be available this month. NXP has provided a video showing an energy-harvesting demo with CHERRY using the JN5168 MCU; view it at www.edn.com/44017920.

NXP Semiconductors,
www.nxp.com

TI MSP430 features separate main and I/O supply rails

The MCUs in Texas Instruments' MSP430F521x/F522x family feature a main supply rail (1.8 to 3.6V) and I/O supply rail (1.8V ±10%). Designed to reduce power requirements for co-processor designs, the dual-rail capability allows for a seamless interface to other devices that have a nominal 1.8V I/O interface without the need for external level translation. The F522x MCUs are available in configurations with four 16-bit timers; a high-performance, 10-bit ADC; two universal serial communication interfaces; hardware multiplier; DMA; comparator; and real-time clock module with alarm capabilities. The F521x devices include all the F522x peripherals except the ADC. TI offers the MCUs in 48- and 64-pin QFN and 80-pin BGA options with up to 128k memory, as well as in a 3.5×3.5-mm YFF package (available in the first quarter). MSP430F521x/F522x MCUs are priced from \$2.05 (1000); samples are immediately available.

Texas Instruments, www.ti.com

DCD's 8051-based IP packs peripherals

Digital Core Design's DT8051, an area-optimized soft core of a single-chip 8-bit embedded microcontroller, can run in very small FPGA devices or can be just a tiny fragment of a system-on-chip ASIC. The DT8051 soft core is 100% binary compatible with the industry-standard 8051 8-bit microcontroller but has a very low-gate-count architecture, providing six 650 ASIC gates for the complete system with peripherals and the DoCD on-chip debugger. The DT8051 includes a two-wire DoCD on-chip debugger, up to eight external interrupt sources, an advanced power-management unit, timers zero and one, I/O bit-addressable ports, full-duplex UART, and interface for external SFR.

Digital Core Design, www.dcd.pl

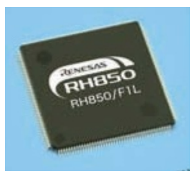
ST extends on-chip memory options for Cortex-based MCUs

STMicroelectronics' STM32 F427 and F437 MCUs combine an ARM Cortex-M4 core with 1 or 2 Mbytes of flash and extra SRAM. The devices are intended for embedded systems that need to run richer applications with extra communication ports, enhanced security, and low power consumption. All of the extended 1- and 2-Mbyte variants have 256-kbyte SRAM, allowing designs using current devices with 1-Mbyte flash and up to 192-kbyte SRAM to move easily to an MCU with higher SRAM if required. The F437 provides enhanced security to protect developer IP and end-user data against unauthorized access. The microcontrollers are slated to enter full production during the first quarter. The price of the STM32F427VGT6 with 1-Mbyte flash and 256-kbyte SRAM in an LQFP100 package is \$7.45 (1000). The price of the STM32F437IIH6 with 2-Mbyte flash, 256-kbyte RAM, and a crypto/hash processor in a UFBGA176 package is \$9.50 (1000).

STMicroelectronics, www.st.com

Renesas ultralow-power series targets automotive-body apps

Renesas Electronics Corp's RH850/F1x series of 32-bit MCUs with on-chip flash for automotive-body applications comprises more than 50 low- to high-end products in three families: the RH850/F1L, RH850/F1M, and RH850/F1H. All share the same CPU core architecture and the same selection of peripheral functions, allowing common software to be used for different system units, and all products in the series incorporate power-supply-shutoff circuit technology for reduced current consumption. The series offers on-chip flash capacity from 256 kbytes to 8 Mbytes. Dual-core versions are also planned to be available in the RH850/F1H group. Samples of the RH850/F1L are scheduled to be available in the second quarter. Mass production of the RH850/F1L is scheduled to begin in 2014.



Renesas, am.renesas.com

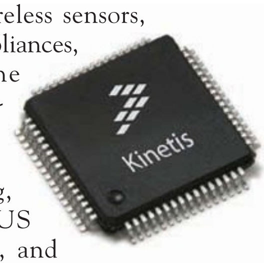
Maxim adds single-chip protection for portable financial systems

Maxim Integrated's MAX32590, based on the ARM926EJ-S processor core, provides improved security features targeting the latest security standards for financial terminals and new generations of trusted devices, such as multimedia-enabled, portable EFT-POS terminals. The MAX32590, the latest member of Maxim's DeepCover security products, combines enhanced security features with more connectivity options. With new features for external memory encryption and integrity checking, the device is designed to simplify system integration as well as provide better IP protection and stronger overall protection against attacks. The chip is available now in production quantities. Maxim also offers a financial-terminal reference design based on the MAX32590.

Maxim, www.maximintegrated.com

Freescale sub-GHz wireless MCU has 32-bit core

The Kinetis KW01 wireless MCU from Freescale Semiconductor Inc is a high-performance radio capable of up to 600 kbits/sec using complex modulation schemes (GFSK, MSK, GMSK, and OOK). The radio operates at multiple frequencies in the range of 290 to 1,020 MHz, supporting ISM bands in many regions of the world. For applications connecting wireless sensors, controls, displays, appliances, and machinery, the KW01 can support proprietary protocols as well as such standards as IEEE 802.15.4e/g, 6LoWPAN, WMBUS (EN13757-4), KNX, and Echonet. The MCU is based on an ARM Cortex-M0+ processor running up to 48 MHz with 128 kbytes of flash and 16 kbytes of SRAM, consuming as little as 40 µA/MHz in typical conditions. Volume production is expected in the first quarter.



Freescale Semiconductor, www.freescale.com

Atmel Cortex-M4-based MCUs boost efficiency

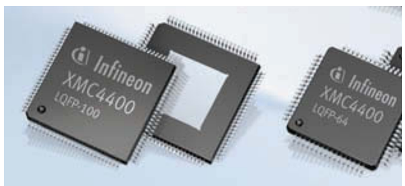
Atmel Corp's SAM4L ultralow-power MCUs, based on the ARM Cortex-M4 processor, offer ultralow-power operation, requiring only 90 µA/

MHz in active mode, 1.5 µA in sleep mode with full RAM retention, and 700 nA in backup mode. Intended for portable and battery-powered designs targeting industrial, medical, and consumer applications, the devices combine 48-MHz operation with 128- to 256-kbyte flash; 32-kbyte SRAM; audio DAC; 15-channel, 12-bit ADC; DAC; multiple interface options; 4×40-segment LCD controller; and 32-channel capacitive-touch controller. Priced at $3.90 to $4.12 (1000), the devices are available in a peripheral-limited LS series and a fully configured LC series, and in 48-, 64-, and 100-pin options for both QFP and QFN packages. The SAM4L-EK evaluation kit is available now.

Atmel, www.atmel.com

Infineon expands XMC4000 family with high-res PWM

Infineon Technologies AG has added three performance classes in its XMC4000 microcontroller family, which targets industrial applications and is based on the ARM Cortex-M4. The XMC4400, XMC4200, and XMC4100 are the first Cortex-based microcontrollers to offer a high-resolution pulse-width-modulation unit, according to Infineon. With a PWM resolution of 150 psec, they are suited for digital power conversion in inverters as well as switching and uninterruptible power supplies. Other applications include I/O units in automation, human-machine interfaces, and logging and control systems. Samples of all three series are available. High-volume production is scheduled to start at the end of the second quarter.



Infineon Technologies,
www.infineon.com

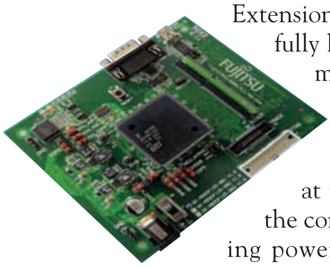
ARM 64-bit Cortex-A50 serves single-processor or multicore apps

ARM Ltd's 64-bit Cortex-A50 processor series comprises the Cortex-A57, targeting high-performance applications, and the Cortex-A53, ARM's most power-efficient application processor. The cores offer higher performance for ARMv7

32-bit code in the AArch32 execution state while also supporting 64-bit data and larger virtual addressing space in the AArch64 execution state. Accordingly, ARM expects the Cortex-A50 processor series to drive a seamless transition from 32- to 64-bit applications and to offer scalability for emerging mobile-computing clients and future "superphones." The processors can operate both in single-processor configurations and in ARM's multicore, big.Little processor configuration, which lets applications use the optimum processor for each task.
ARM,
www.arm.com

Fujitsu touts hardware security for automotive instrument cluster

Fujitsu Semiconductor Europe has expanded its scalable lineup for automotive instrument clusters. The newest member of Fujitsu's FCR4 family, the MB9DF125 Atlas-L, is based on the ARM Cortex-R4 core and includes a Secure Hardware Extension module that is fully hardware-implemented to ensure the highest levels of security. Operating at up to 128 MHz, the core offers processing power of more than 200 Dhrystone Mips, together with 1 Mbyte of flash and 128 kbytes of RAM. Atlas-L will ship in an LQFP-176 package. First samples are available now.



Fujitsu Semiconductor,
www.fme.fujitsu.com

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EDN product mart

This advertising is for new and current products.

SiLabs 8-bit controllers integrate temperature sensors for accuracy

Silicon Laboratories Inc's C8051F39x/7x high-performance 8-bit MCUs integrate a temperature sensor with best-in-class accuracy over an extended range without calibration. The family combines integrated high-performance analog peripherals with a fast 8051 CPU in a compact package. The on-chip temperature sensor provides ±2°C accuracy—five times higher, the company claims, than competing MCUs—in a 30% smaller package. The devices are a first for Silicon Labs MCUs, with 512 bytes of E^2PROM supporting 10 times more write/erase cycles (1 million, versus 100k typical) and faster programming times than standard flash implementations. Pricing (10,000) begins at 98 cents. The C8051F390-A-DK and C8051F370-A-DK development kits are available for $69; the ToolStick370-A-DC daughtercard is available for $9.

Silicon Labs, www.silabs.com

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FRANK W BELL • KYBERNETIX LLC

Nonlinear transmission lines keep developer on the fence

In 1982, I was developing a phone and telemetry system to operate on New Zealand farmers' electrified fences. The controller that generated the jolt was usually a mains-powered pulse generator, and better units produced mostly unipolar pulses of up to 5 kV for a duration of about 20 msec, repeated about once a second—not lethal, but enough to kill any notion of touching the fence again. The high voltages were even effective on unshorn, woolly sheep.

Such a fence behaves as an earth-return transmission line with an impedance of around 600Ω, depending on construction. The system polarity is decided based on resistance to lightning, which usually consists of negative current into the fence from a direct strike, though positive current may come from a strike nearby. The system I was developing used biased blocking diodes to prevent the pulse from frying the electronics (not to mention avoiding the loud click in the ear). Detection of a dc bias on the fence turned on a DTMF decoder to select the receiver.

Field trials were essential. On one farm, the DTMF decoder provided an output burst a couple of times and then died. Testing with a blocking diode and oscilloscope showed a positive pulse of 12 μsec after the negative controller pulse. Assuming a velocity factor of 0.7, that gave a range of 1.25 km, or about three-quarters of a mile. When I checked the fence leakage to ground, however, it was more than 3 kΩ for the whole farm. The controller included a circuit to eliminate positive pulses. How could a low impedance have inverted the pulse polarity?

I drove out in a truck to the 1.25-km distance on the odometer. I didn't see any stray wires going into the ground, a common problem. When I got out of the truck, though, I noticed an audible click with a 1-sec interval.

I took a look at the fence. The farmer had used steel posts and had cut lengths of plastic hose, with a lengthwise slit, for insulators. A thin wire tied the hose to the post. Though there was insulation, the air gap was breaking down with the pulse from the controller and producing a positive polarity reflection. I explained the problem to the farmer, who later installed proper insulators and told me the fence worked "much better now."

After diagnosing the cause of the failure of my prototype electric fence telephone/DTMF controller, I installed additional clamping so that positive pulses would not reach the DTMF decoder. Normally, farmers did their testing without any instruments—though perhaps with rubber gumboots—by touching the fence and a blade of grass, but testing in this environment required battery-powered oscilloscopes, as the voltage on the grounding points could easily exceed the rated insulation of the mains-powered equipment. The educational material for the controller installation made it clear that the controller ground had to be well separated from the ground of the ac mains because of such voltages.

On another farm, connections between phones along the fence were intermittently dropping out between controller pulses. I checked out the fence, which was so rusty that I had to work the alligator clips—with insulated pliers, of course—to get a connection to the metal underneath. The connections between wires were simply loops holding loops. These also were rusty connections, and the arc of the pulse temporarily welded the wires together. Poor connections also cause AM radio interference when they get rusty. The farmer replaced the rusty fence, which was becoming unreliable anyway.

In order to examine the high-voltage pulses, we modified a Heathkit TV high-voltage probe using a capacitor made from car-ignition cable with a metal conductor, a braid on the outside, and a divider and a compensation circuit to correct the square waves from a calibration source (tube scope) of higher-than-normal voltage. The Tektronix EHT probe would have been better, but it wasn't affordable.

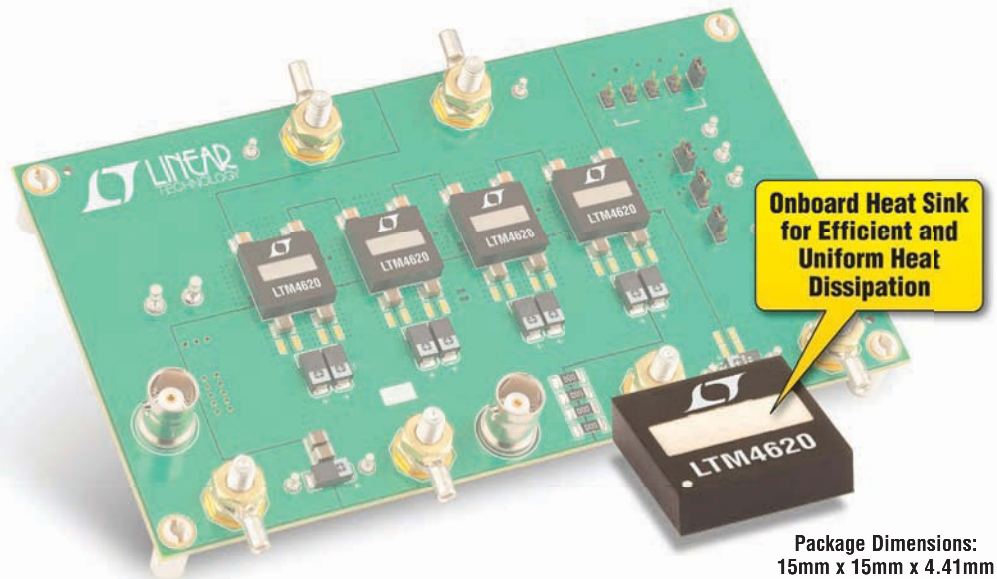
The patent for the telemetry system eventually expired without resulting in a successful product. EDN

Frank W Bell is president of Kybernetix (Clifton, NJ).

DANIEL VASCONCELLOS

Single 26A or Dual 13A µModule Regulator

Scalable to 100A with Four LTM®4620 µModule® Regulators



Package Dimensions:
15mm x 15mm x 4.41mm

Proof of Performance


High Efficiency


Precision Current Sharing*


Fast Short Circuit Protection


Excellent Thermal Performance**

Features

- Dual 13A or Single 26A Complete Step-Down Regulator with Inductors, MOSFETs and DC/DC Controller
- $4.5V \le V_{IN} \le 16V$
- $0.6V \le V_{OUT} \le 2.5V$
- Internal Temperature Sense
- ±1.5% V_{OUT} Accuracy Over Temperature Including Remote Sense Amplifier
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